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Features
- Supports Xilinx® Zynq™-7000 EPP and 7 Series, Spartan®-6, Virtex®-6 and older Xilinx FPGA families
- Compliant to ISO11898-1, CAN 2.0B and CAN 2.0A protocol specifications
- Supports both, standard (11-bit identifier) and extended (29-bit identifier) frames
- Supports bit rates up to 1 Mbps
- Receive message FIFO (up to 63 messages)
- Transmit message FIFO (up to 31 messages)
- Four programmable acceptance filters for message filtering
- Supports bit timing requirements, hard synchronization and resynchronization, bus arbitration, automatic retransmission in case of error or lost arbitration, automatic Bus-Off recovery, error handling and fault confinement, automatic CRC code generation and check up
- Support for auto bit rate detection (bus listening mode)
- Supports internal loop-back mode

Table 1: Example Implementation Statistics for Xilinx® FPGAs

<table>
<thead>
<tr>
<th>Family (Device)</th>
<th>Fmax (MHz)</th>
<th>Fmax (MHz)</th>
<th>LCs</th>
<th>Slices(^1) (FFs/LUTs)</th>
<th>LUTRAM</th>
<th>IOB(^2)</th>
<th>BRAM</th>
<th>MULT/DSP48/E</th>
<th>DCM/CMT</th>
<th>GTx</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>can_clk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spartan®-3</td>
<td>111</td>
<td>33</td>
<td>1649</td>
<td>733 (545/1015)</td>
<td>-</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE14.1</td>
</tr>
<tr>
<td>(XC3S200-4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Spartan®-6</td>
<td>176</td>
<td>70</td>
<td>1990</td>
<td>311 (529/702)</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE14.1</td>
</tr>
<tr>
<td>(XC6SLX45-3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Artix™-7</td>
<td>216</td>
<td>96</td>
<td>2253</td>
<td>352 (529/690)</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE14.1</td>
</tr>
<tr>
<td>(XC7A50T-3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Kintex™-7</td>
<td>240</td>
<td>115</td>
<td>2720</td>
<td>425 (529/785)</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE14.1</td>
</tr>
<tr>
<td>(XC7K70T-3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex®-7</td>
<td>337</td>
<td>145</td>
<td>2515</td>
<td>393 (529/791)</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE14.1</td>
</tr>
<tr>
<td>(XC7VX330T-3)</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

Notes:
1) Assuming: 8 TX buffers, 32 RX buffers, disabled acceptance filtering
2) Assuming TX and RX signals are routed off-chip
Features (cont)

- Readable Error Counters
- Supports transmission abort
- Register interface ARM® AMBA® AXI4-Lite 32-bit interface
- Interrupt processing for all errors and message exchange
- Low CPU overhead
- External CAN bus transceiver required
- Fully synchronous, field proven design
- Parametrizable VHDL design that allows customization and can be tailored to fulfill your needs
- Fully functional core available under evaluation license
- Prepared for Xilinx Platform Studio (XPS) and the EDK

Applications

The logiCAN core can be used in wide range of applications, whereas the CAN protocol takes place due to its speed, high security and efficiency. This range of applications embraces the simple multiplex wiring systems as well as the highly integrated automotive or building management applications.

Small logiCAN size enables multiple CAN controller implementations on a single FPGA.
General Description

The logiCAN core supports ISO11898-1, CAN 2.0B and CAN 2.0A specified protocol functions. It provides all features expected from the standard CAN controllers including: global masking (acceptance filtering) with 4 masks for the Standard or Extended CAN frames, fault confinement, stuff bit generation, CRC and arbitration handling. The ISO11898-1 TTC (time triggered communication) option is not supported.

What makes logiCAN different from standard CAN solutions are its highly automated message handling. The CPU, released from continuous CAN controller handling, can be used for other system tasks. It is extremely important for efficient low-cost systems.

Simple fill of the TX buffer (TX FIFO) starts a frame (message) transmission and all further actions, such as bus monitoring, arbitration loss and retransmission in the bus error case are handled by the logiCAN with no CPU interventions. Multiple RX buffers (RX FIFO) ensure full frame reception, even at the highest baud rates. Only error-free, mask complying (pass-through acceptance filters) messages are stored, while others are checked, acknowledged and simply discarded. In mixed CAN networks, with standard and extended frames present on the same bus, an automatic frame type recording is assured.

Functional Description

The logiCAN core consists of: Regs module, Data Control module, Protocol Control module and Bit Timing module. The internal structure is shown in the block diagram - Figure 1.

Regs module

The Regs module features all logiCAN’s registers. Core’s operations are controlled and monitored by Control and Status registers. Set-up registers for message filtering, as well as error counters and bit timing registers, are also parts of the Regs module.

Data Control module

This module accepts the serial input from the CAN bus, parses it, and stores into internal buffers. Data from TX buffer is loaded into output shift register. RX and TX FIFOs are realized in a single Block RAM. The number of TX and RX buffers is configurable. CPU has 32-bit wide access to FIFO, while the CAN control logic has 8-bit wide access to this Block RAM. Each of 31 TX and 63 RX buffers uses 16 bytes of FIFO memory space. The RX/TX buffer (one FIFO location) is visible as four 32-bit storage locations to the CPU. TX buffer is visible at the beginning of FIFO memory space, while the RX buffer immediately follows. There must be at least one TX buffer and one RX buffer. Both, RX and TX buffers are independently handled in a circular buffer fashion. Acceptance filtering (global masking filters) for Standard and Extended frames are provided. The CRC submodule generates and checks an appropriate CRC sequence. Interrupt processing for all errors and message exchange is done in Interrupt sub-module.

Protocol Control module

The Control module is the core of the logiCAN. It implements the majority of control logic: bus states control, CAN frame parsing, error recognition, receive and transmit logic and complete fault confinement supporting logic.

Bit Timing module

CAN networks are built by a number of network nodes. Since network node is clocked with its own oscillator, the clock phase shift is present. The CAN protocol specifies a special synchronization algorithm to compensate phase shift. Bit timings are programmable (SYNC, SETUP and HOLD), the sampling point is adjustable.
Core Modifications

VHDL constants, listed in Table 6, enable an easy customization of the logiCAN architecture.

Table 2: logiCAN VHDL configuration parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_ID_MASKING</td>
<td>0, 1 – Disable/Enable Acceptance Filtering (global masking filters)</td>
</tr>
<tr>
<td>C_NUM_RX_BUFS</td>
<td>1 – 63</td>
</tr>
<tr>
<td>C_NUM_TX_BUFS</td>
<td>1 – 31</td>
</tr>
<tr>
<td>C_TQ_PRESCALE</td>
<td>0 – 15</td>
</tr>
</tbody>
</table>

Although the logiCAN has been constructed compliant to the ISO11898-1, CAN 2.0B and CAN 2.0A protocol specifications and for the CAN network analysis, there may be instances where the source code modification is necessary. Please contact Xylon for any required modifications.

Core I/O Signals

The core signal names are shown in Figure 1 and described in Table 5.

Table 3: Core I/O Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Signal Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>can_clk</td>
<td>Input</td>
<td>Clock for CAN state machine</td>
</tr>
<tr>
<td>rx</td>
<td>Input</td>
<td>Receive input from CAN transceiver</td>
</tr>
<tr>
<td>tx</td>
<td>Output</td>
<td>Transmit output to CAN transceiver</td>
</tr>
<tr>
<td>frst_err</td>
<td>Output</td>
<td>First CAN bus error signal</td>
</tr>
</tbody>
</table>

Verification Methods

The logiCAN has been developed as part of a larger design. It is verified in both ways: functional simulation and it is field tested/proved in a large-scale production. Older versions of this core have been successfully used in Virtex/Spartan2, XC4000 and Spartan FPGA families. Functional verification is performed by using C language Bosch referent CAN model as gold reference with stimulus generated by Bosch verification tests as well.

Provided automated VHDL test-bench can be used for the basic functionality test, i.e. simple frame exchange. It is primarily aimed for an integration and software logiCAN initialization check up.

Recommended Design Experience

The user should have experience in the following areas:
- ISO11898-1, CAN 2.0B and CAN 2.0A protocol specification
- ModelSim
- Xilinx XPS tool
Available Support Products

Xylon logicBRICKSTM IP cores can be evaluated on the logiCRAFT-CC Xylon development platform, which is designed especially for developers working in the fields of multimedia and infotainment. This platform demonstrates modularity on all levels: software, board, FPGA, and IP cores. The platform makes excellent development tool particularly appropriate for the development of embedded systems with strong graphics capabilities. The logiCRAFT-CC board includes CAN transceivers and connectors for easy interconnections with CAN networks.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon’s IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

CAN in Automation (CiA)

It is a non-profit trade association of international users and manufacturers. CiA provides technical, product and marketing information regarding Controller Area Network applications. Can be contacted directly at:

CAN in Automation e.V.
E-mail: headquarters@can-cia.de
Phone: +49-9131-69086-0
Fax: +49-9131-69086-79
URL: www.can-cia.com/

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.01</td>
<td>20.03.2006</td>
<td>Initial Xylon release – new doc template</td>
</tr>
<tr>
<td>3.00</td>
<td>20.06.2012</td>
<td>New doc template. New features added.</td>
</tr>
</tbody>
</table>