Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs constraint files
Reference Designs & Application Notes	Contact info@logicbricks.com
Simulation Tool Used	
Mentor Graphics' Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC and 7 series FPGA families
- Compliant with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard
- On-the-fly video encoding to Motion JPEG stream
- JPEG headers inserted on-the-fly in the compressed video output
- Configurable video compression factor
- Video input/output resolutions up to 2048x2048
- Supported pixel formats: YUV 4:2:0 and YUV 4:2:2
- High data throughput at the video input, i.e. 150 MPix/s when running at 150 MHz (1080p@60fps support)
- AMBA® AXI4-Stream compliant video input and video output (MJPEG)
- No-programming required; a single control signal input enables/disables the AXI4-Stream MJPEG output
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Available IP core deliverables prepared for the Xilinx Vivado® Design Suite
- IP deliverables include documentation and technical support
- Plug and Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiJPGD Multi-Channel JPEG Decoder and the logiISP Image Signal Processing Pipeline

Table 1: Example Implementation Statistics for Xilinx FPGAs

Family (Device)	Fmax (MHz) clk	LUT	FF	IOB	BRAM	DSP48	PLL/ MMCM	BUFG/ BUFR	GTx	Design Tools
Zynq-7000 (XC7Z020-1)	150	3240	1969	0	16	30	0	0	0	Vivado 2019.2
Artix®-7 (XCA200T-2)	220	3104	1978	0	16	30	0	0	0	Vivado 2019.2
Kintex®-7 (XC7K325T-2)	220	3105	1970	0	16	30	0	0	0	Vivado 2019.2

1) Assuming the following configuration: maximum resolution 2048, video format YUV4:2:2

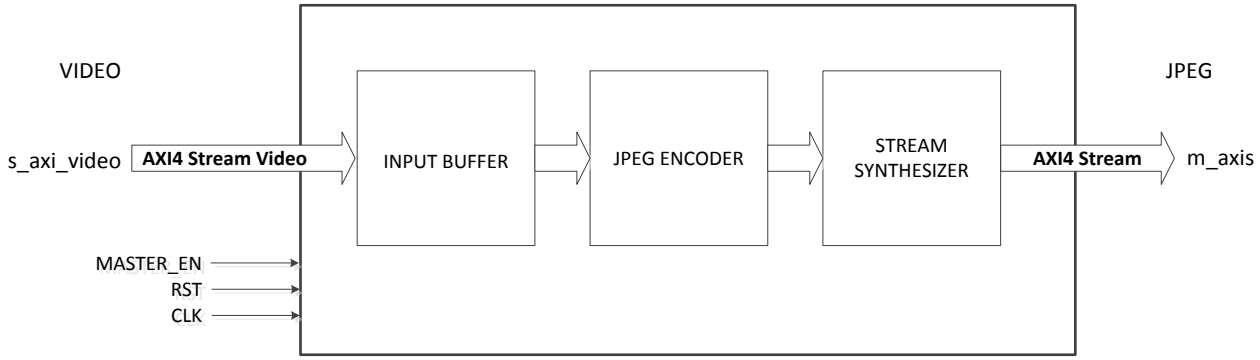

Figure 1: logiJPGE Architecture

Applications

The logiJPGE IP core can be used in all applications that require JPEG or MJPEG video compression. It is particularly well-suited for video over IP applications like:

- Various camera designs with an integrated video compression feature
- Four-Camera Surround View and other Advanced Driver Assistance (ADAS)
- Multi-camera surveillance systems
- …

General Description

The logiJPGE Motion JPEG Encoder is Xylon logicBRICKS IP core for still image and video compression applications on Xilinx All Programmable SoC and FPGA devices. It includes all logic blocks necessary for quick implementations of AMBA AXI4 streaming based SoC architectures and enables on the fly JPEG compression of input video with resolutions up to 2048 x 2048 (including the full HD video at 60 fps – 1080p@60).

At the center of the logiJPGE IP core is the ISO/IEC 10928-1 JPEG standard compliant Baseline DCT encoder block that works with the YUV (4:2:0 and 4:2:2) video formats and supports all standard features such as quantization, Huffman encoding, ZIG-ZAG and automatic insertion of JPEG headers. The JPEG encoder block is coupled with the AMBA AXI4-Stream compatible stream logic blocks that handle video data transfers from the video source towards the logiJPGE IP core and compressed JPEG stream transfers from the IP core towards next stages in the video processing pipeline.

The logiJPGE IP core's input interface is compatible with the Slave AXI4-Stream Video Input Interface protocol and its output is compatible with the Master AXI4-Stream Output Interface. In typical IP applications the MJPEG encoded video output is transferred to remote video systems, i.e. over the Ethernet network, to be decoded by an appropriate JPEG decoder, such as the logiJPGD Multi-Channel Motion JPEG Decoder from Xylon's logicBRICKS IP library. With an appropriate storage control IP core, i.e. Xilinx AXI DMA IP core, the logiJPGE output can be also stored directly to local memory.

A variety of interrelated factors affect the achievable logiJPGE IP core's performance. Targeted Xilinx All Programmable logic, the overall SoC design's complexity and the input video resolutions and frame rates are some of the more common parameters that affect a core's performance. The logiJPGE IP core is carefully architectured to provide high data throughput even in low and mid-range FPGAs, i.e. 150 MPix/s when running at 150MHz. Such data throughput enables smooth encoding of one 1080p@60 or multiple 720p@30 HD video inputs.

The logiJPGE is fully embedded into Xilinx Vivado IP implementation tools, hides complexity from the end user, and its integration with the on-chip AMBA AXI4-Stream bus is easy. The logiJPGE does not need any initialization and software support, and it can work even in systems without a CPU. Parametrizable VHDL

design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiJPGE can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores.

If you are interested in the logiJPGE IP evaluation, please contact info@logicbricks.com.

Application Example

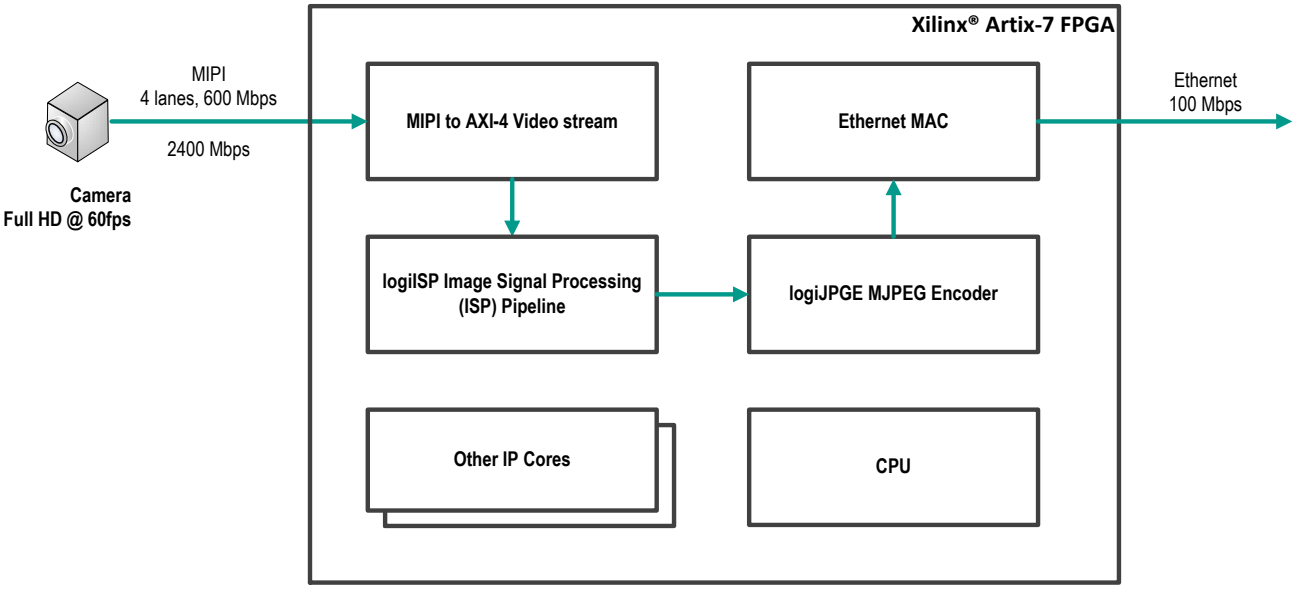

Figure 2: logiJPGE Use Case Scenario Example

Figure 2 illustrates an example of the logiJPGE IP core use in the Ethernet based camera application. A full HD camera sensor, which is connected to the Xilinx Artix®-7 FPGA through the MIPI Camera Serial Interface CSI-2, sources high resolution video with the 60fps refresh rate. The captured video is converted to the AXI4-Stream compliant streaming video and digitally processed and enhanced by the logiISP Image Signal Processing (ISP) Pipeline IP core from Xylon. The original input video data bandwidth of 2400 Mbps is too high for data transfers through the 1 Gbps Ethernet network, which is a very common interface in this type of camera applications. The logiJPGE IP core compresses the input video and decreases the required data bandwidth of the communication channel to only 100 Mbps. The video payload needs to be further packed into UDP packets prior to transmission. The described video processing mechanism actually enables transfers of multiple high resolution video channels through a single 1 Gbps Ethernet connection.

Functional Description

The logiJPGE consists of the following blocks: Input Buffer, JPEG Encoder and Stream Synthesizer

Input Buffer

Input Buffer accepts input AXI4-Stream, stores minimum 8 (for YUV4:2:0) or 16 (for YUV4:2:2) lines and feeds the JPEG Encoder with 8x8 Minimum Coded Unit (MCU) ready for DCT.

JPEG Encoder

The JPEG Encoder is compliant with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard. It encodes (compresses) the YUV video input and provides the compressed JPEG coded YUV video output.

Stream Synthesizer

JPEG Synthesizer adds JPEG header and generates JPEG stream from the encoded video data stream.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado Design Suite (IP Integrator), which allows the user to take full control over IP configuration parameters. Table 2 outlines some of important logiJPGE configuration parameters selectable prior to the VHDL synthesis.

Table 2: logiJPGE Configuration Parameters

Parameter	Description
C_COMPRESSION	Compression factor, from 1 (max. compression – min. quality) to 100 (max. quality – no compression).
C_MAX_HRES	Maximum input horizontal resolution: 1024 or 2048.

The logiJPGE has been constructed with regard to adaptability to various video applications. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach the optimal use of the logiJPGE core and/or to implement some of your specific functions, you can order the source code or allow us to tailor the logiJPGE to your requirements. The logiJPGE VHDL source code is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in the Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global reset input
CLK	Input	Main clock input
Video Input Interface		
AXI4 Stream Video Interface	Bus	Video Input AXI4 stream video interface
Output Interface		
AXI4 Stream Master Interface	Bus	JPEG Output AXI4 stream interface
Auxiliary Signals		
MASTER_EN	Input	Enable output interface

Verification Methods

The logiJPGE is fully supported by the Xilinx Vivado IP Integrator integrated software solution. This tight integration tremendously shortens IP integration and verification. The logiJPEG full implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiJPGD Multi-Channel Motion JPEG Decoder is JPEG standard Baseline DCT compliant decoder IP core for still image and video decompression applications on Xilinx All Programmable SoC and FPGA devices. This IP core is specially designed for video over IP applications where the video payload from multiple video channels comes in a non-guaranteed order and encapsulated in network frames, i.e. the Ethernet UDP packets.

To learn more about the Xylon logiJPGD IP core, contact Xylon or visit the web:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiJPGD.aspx

The logiJPGE IP core is often used with the logiISP Image Signal Processing (ISP) Pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx All Programmable devices.

To learn more about the Xylon logiISP IP core, contact Xylon or visit the web:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiISP.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.0	02.11.2015.	Initial. Not public.
1.0	10.01.2018.	The first public release. Updated Table 1.
1.0	03.07.2020.	Updated Table 1.