Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	
Verification	
Reference Designs & Application Notes	
Additional Items	Xylon logiCRAFT-CC board
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- High performance multi-port memory controller designed for Xilinx® Spartan®-6 FPGA
- Utilizes up to four Xilinx Memory Controller Blocks (MCB) and supports DDR/DDR2/DDR3/LPDDR
- Achievable memory bandwidths of up to 6.4GBytes/sec
- Supports total of 16 system ports and up to 8 simultaneous memory accesses
- Supports ARM® AMBA® AXI4, CoreConnect PLB, Xilinx Cache Link XCL, Xilinx Native Port Interface NPI, and Xylon Memory Bus (XMB)
- Each system port has configurable data width (32, 64 and 128-bit)
- Each system port can be configured as a read-only, write-only or bidirectional read-write port
- Independent write and read priority arbitrations
- Each system port can be configured to support either the AXI4 or (XMB) bus standard
- Supports AXI4 WRAP burst up to 16 beats and the INCREMENTAL burst up to 64 beats

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) clk	LCs	Slices[1,6] (FFs/ LUTs)	IOB	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
Spartan®-6[2] (XC6SLX45T-3)	137	4902	766 (589/1461)	0	0	0	0	0	N/A	ISE® 14.4
Spartan®-6[3] (XC6SLX45T-3)	137	14835	2318 (1586/3964)	0	0	0	0	0	N/A	ISE® 14.4
Spartan®-6[4] (XC6SLX45T-3)	137	11226	1754 (1209/3193)	0	0	0	0	0	N/A	ISE® 14.4
Spartan®-6[5] (XC6SLX150T-3)	137	22125	3457 (2425/6419)	0	0	0	0	0	N/A	ISE® 14.4

Notes:
1) Assuming the following configuration: 4 XMB, 4 AXI and 1 PLB ports used
2) Assuming the following configuration: 1 MCB connected, with single 128-bit link, internal data width is 128-bit
3) Assuming the following configuration: 2 MCBs connected, both with double 64-bit link, internal data width is 64-bit
4) Assuming the following configuration: 2 MCBs connected, both with single 128-bit link, internal data width is 128-bit
5) Assuming the following configuration: 4 MCBs connected, all with single 128-bit link, internal data width is 128-bit
6) Slice consumption decreases with lower number of connected user ports

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved

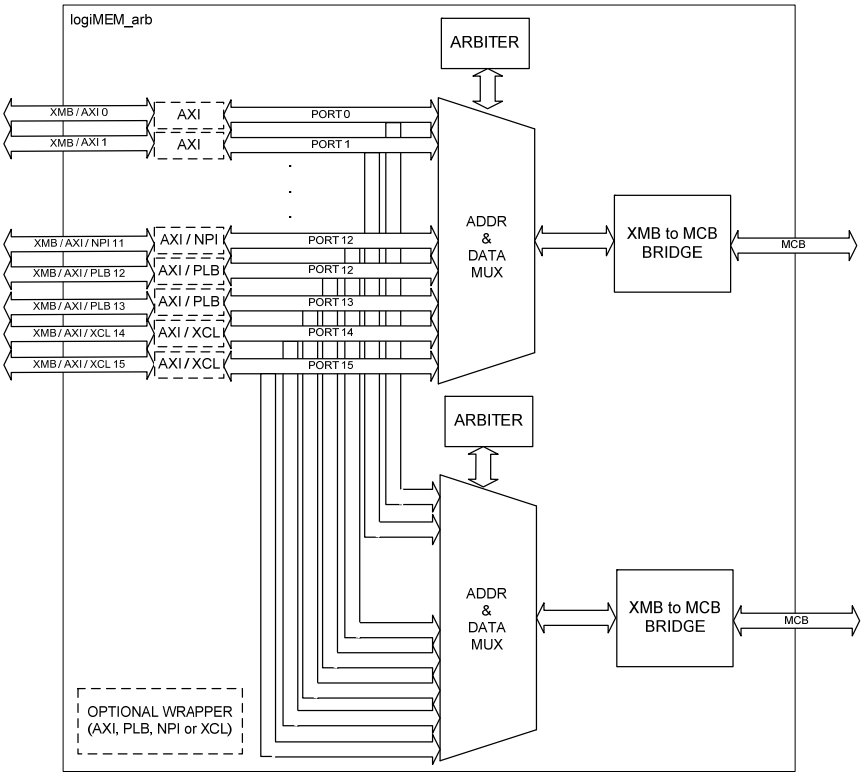

Figure 1 : logiMEM_arb Architecture (configuration with 2 MCBs)

Features (cont)

- Includes two Xilinx PLBv4.6 compliant ports
- Includes two XCL compliant ports for Xilinx MicroBlaze™ 32-bit cache interface connections
- One of the two PLB ports and both XCL ports support asynchronous MicroBlaze CPU clock speeds
- MicroBlaze PLB v46 slave interface (MBSPLB) – single-beat access is supported
- One port can be configured as the NPI port
- Supports single-beat and burst transaction on the PLB bus
- Programmable burst transfers from 1 to 64 words (32, 64 or 128-bit) on XMB
- Burst length applies for both Read and Write cycles
- Interface with the MCB through either single 64-bit, double 64-bit or single 128-bit data bus
- Round Robin and Fixed Priority arbitration algorithms configurable for each port
- Parametrical VHDL design allowing tuning of slice consumption and features set
- Synthesizable VHDL source code
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as:
  - logiWIN Versatile Video Input
  - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
  - logi3D Scalable 3D Graphics Accelerator
  - logiCVC-ML Compact Multilayer Video Controller

Applications

- Car Infotainment and Telematics
- Industrial test equipment, surveillance, HMI…
- Medical equipment
- Aerospace and Defense devices, Electronic Gadgets, etc.

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved

General Description

The logiMEM_arb Memory Controller and Arbiter IP core from Xylon's logicBRICKS IP library allows users to easily connect different SDRAM (Synchronous Dynamic Random-Access Memory) memories to the Xilinx Spartan-6 FPGA chip. The IP core fully utilizes Xilinx's embedded Memory Controller Blocks (MCB) hard IP cores and enables the maximum achievable memory bandwidths of up to 6.4 GBytes/sec.

The logiMEM_arb memory controller IP core supports up to 16 ports for on-chip processor and peripheral IP connections, and by means of memory interleaving, simultaneous memory accesses of up to 8 IP cores. The simultaneous memory accesses greatly improve memory bandwidth utilization of external SDRAM devices, and in well tuned systems, the memory bandwidth utilization can reach more than 90% of the theoretically available memory bandwidth. The IP core can use all available MCBs within the certain Xilinx Spartan-6 chip device.

The logiMEM_arb Memory Controller and Arbiter's system ports for IP connections are very programmable. Users can configure the system ports to support the following on-chip bus standards: ARM AMBA AXI4, CoreConnect Processor Local Bus (PLB), Xilinx Cache Link for Xilinx's soft-CPU MicroBlaze cache interface, Xilinx Native Port Interface (NPI) and the lightweight Xylon Memory Bus (XMB).

Functional Description

The Figure 1 presents internal logiMEM_arb architecture. The logiMEM_arb functional blocks are: Arbiter, Address and Data Multiplexer, XMB to MCB Bridge and Bus wrappers (PLB, XCL, AXI and NPI).

Arbiter

The Arbiter functional block arbitrates between 16 available user ports and grants memory access to the selected user port, independently for read and write operations (AXI4 ports support simultaneous read and write operations). Separate arbiters are used for reads and writes. The number of instantiated arbiters in specific logiMEM_arb IP core's configuration complies with the number of used MCB blocks.

Address and Data Multiplexer

The Address and data multiplexer block, which is controlled by the Arbiter block, routes selected user ports qualifier signals and data to the XMB to MCB bridge. The number of instantiated Address and Data Multiplexer blocks complies with the number of used MCB blocks.

XMB to MCB Bridge

The XMB to MCB bridge controls operations of the MCB hard-IP block: write and read cycles, termination of AXI and XMB transfers, maintenance of write and read MCB's FIFO levels, and conversions of the AXI and the XMB bus transfers to the MCB transfers. Configuration with more than one MCB instantiates the same number of XMB to MCB bridge blocks. Each XMB to MCB bridge communicates with all other instantiated XMB to MCB bridges to avoid collisions between the data routed to the same user port. The bridge implements data width conversion function that takes care on the configured Endianness parameter and enables narrow masters to access memory through wider internal bus.

Wrappers (PLB, XCL, AXI and NPI)

Internal logiMEM_arb architecture is designed to arbitrate between XMB and AXI transfers. Optional bus wrappers are blocks for conversion of various data protocols (PLBv4.6, AXI4, XCL and NPI) to Xylon Memory Bus (XMB) protocol. AXI wrapper does not incur any penalty on slice consumption nor latency.

Core Modifications

Depending on the purchased license's type, the core is supplied in either an encrypted source or a full source VHDL format compatible with the Xilinx Platform Studio. Many logiMEM_arb configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved

Table 2: logiMEM_arb VHDL configuration parameters

Parameter	Description
C_INT_MEM_DATA_WIDTH	Internal data bus width (64, 128)
C_NUM_OF_MCBS	Number of connected MCBs
C_MCB_PAIR	Connection to MPMC with single 64-bit or dual 64-bit MCB link
C_INTERLEAVE_LENGTH	Number of words (C_INT_MEM_DATA_WIDTH-bit words) after which user port will access different MCB
C_USERN_PORT_TYPE	User port N type (XMB, AXI, NPI, PLB, XCL)
C_USERN_DATA_WIDTH	User port N data width
C_USERN_BURST_WIDTH	Maximal burst size on N port
C_USERN_PRIORITY	User port N priority
C_USERN_SUPPORTS_READ	User port supports read
C_USERN_SUPPORTS_WRITE	User port supports write

The logiMEM_arb has been designed with regard to adaptability to various data transfer protocols and memory access. However, there may be instances where source code modification is necessary. Therefore, if customer wishes to reach the optimal use of the logiMEM_arb core for specific application or to supplement some specific functions, Xylon can tailor logiMEM_arb according to customer requirements.

Core I/O Signals

The core signal I/O has not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	System reset
CLK	Input	Clock
MCB0_init_done	Input	Initialization done signal from MCB0
MCB1_init_done	Input	Initialization done signal from MCB1
MCB2_init_done	Input	Initialization done signal from MCB2
MCB3_init_done	Input	Initialization done signal from MCB3
XMB signals		
userN_req	Input	User port XMB request
userN_wr	Input	User port XMB write
userN_ack	Output	User port XMB acknowledge
userN_addr	Input	User port XMB address
userN_data	Input	User port XMB write data
userN_data_be	Input	User port XMB write data byte enable
userN_wrack	Output	User port XMB write acknowledge
userN_burst_len	Input	User port XMB write and read burst length
userN_data_out	Output	User port XMB read data
userN_data_valid	Output	User port XMB read data valid

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved

Signal	Signal Direction	Description
System Interfaces		
AXI slave	Bus	AXI interface. Refer to ARM AMBA AXI4 Protocol Version specification
SPLB slave	Bus	PLB interface. Refer to Xilinx-IBM Core connect specification
MBSPLB slave	Bus	PLB interface. Refer to Xilinx-IBM Core connect specification
MCH0	Bus	XCL interface. Refer to MicroBlaze Processor Reference Guide
MCH1	Bus	XCL interface. Refer to MicroBlaze Processor Reference Guide
MCB0	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB0_P	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB1	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB1_P	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB2	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB2_P	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB3	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide
MCB3_P	Bus	MCB interface. Refer to Spartan-6 FPGA Memory Controller User Guide

Verification Methods

The logiMEM_arb is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiMEM_arb implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS IP cores can be evaluated on the logiCRAFT-CC Companion Chip Xylon development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. These platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. The logiCRAFT-CC platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiCRAFT-CC.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

This publication has been carefully checked for accuracy. However, Xylon does not assume any responsibility for the contents or use of any product described herein. Xylon reserves the right to make any changes to product without further notice. Our customers should ensure that they take appropriate action so that their use

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved

of our products does not infringe upon any patents. Xylon products are not intended for use in the life support applications. Use of the Xylon products in such appliances is prohibited without written Xylon approval.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.03.	06.04.2011.	Initial Xylon release – new doc template
1.04.	24.01.2012.	New version
2.00.	18.04.2013.	Independent write and read arbitration support, updated resource table, new user parameters

Copyright © Xylon d.o.o. 2001-2013 All Rights Reserved