

Xylon d.o.o.

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Features

- Supports versatile digital video input formats:
 - ITU656 (PAL,NTSC) or ITU1120; 8/10-bit
 - RGB
- Built-in YCbCr to RGB converter
- Embedded image color enhancements: brightness, contrast, hue, saturation
- Real-time video scale-up (zoom in) up to 64x
- Real-time video scale-down (zoom out) down to 16x
 - Lossless scaling down to 2x, or 4x in cascaded mode
- Supports video input cropping and smooth image positioning
- Configurable register interface; CoreConnect™ OPB or PLB interface
- Configurable video memory interface: XMB (Xylon Memory Bus) or CoreConnect™ PLBv46
- Compressed stencil buffer in BRAM (mask over output buffer)
- Supports Pixel Alpha blending
- Maximum input and output resolutions are 2048 x 2048 pixels
- Provides "Bob" and "Weave" deinterlacing algorithms
- Supported Big and Little Endianness
- Double or triple buffering for video flicker prevention

Core Facts	
Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	Reference design simulation
Reference Designs & Application Notes	XPS reference design
Additional Items	Xylon hardware platforms: logiCRAFT6, logiCRAFT-CC and logiTAP SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LCs	Slices ¹ (FFs/ LUTs)	IOB ²	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	vcclk	rcclk									
Spartan®-3E (XC3S1200E-5)	115	115	150	2165	962 (972/985)	28	0	3	6	0	N/A	ISE® 11.4
Spartan®-6 (XC6SLX16-2)	140	140	200	2304	360 (818/660)	28	0	3	6	0	N/A	ISE® 11.4
Virtex®-5 (XC5VLX30-3)	250	250	350	3091	483 (866/768)	28	0	2	6	0	N/A	ISE® 11.4
Virtex®-6 (XC6VLX75T-3)	270	270	445	2297	359 (818/646)	28	0	3	6	0	N/A	ISE® 11.4

Notes:

1) Assuming the following configuration: RGB input, RGB888 output, 32-bit PLB registers interface and memory interface, scaling with MULT/DSP48s

2) Assuming only video inputs are routed off-chip, register and memory interfaces are connected internally

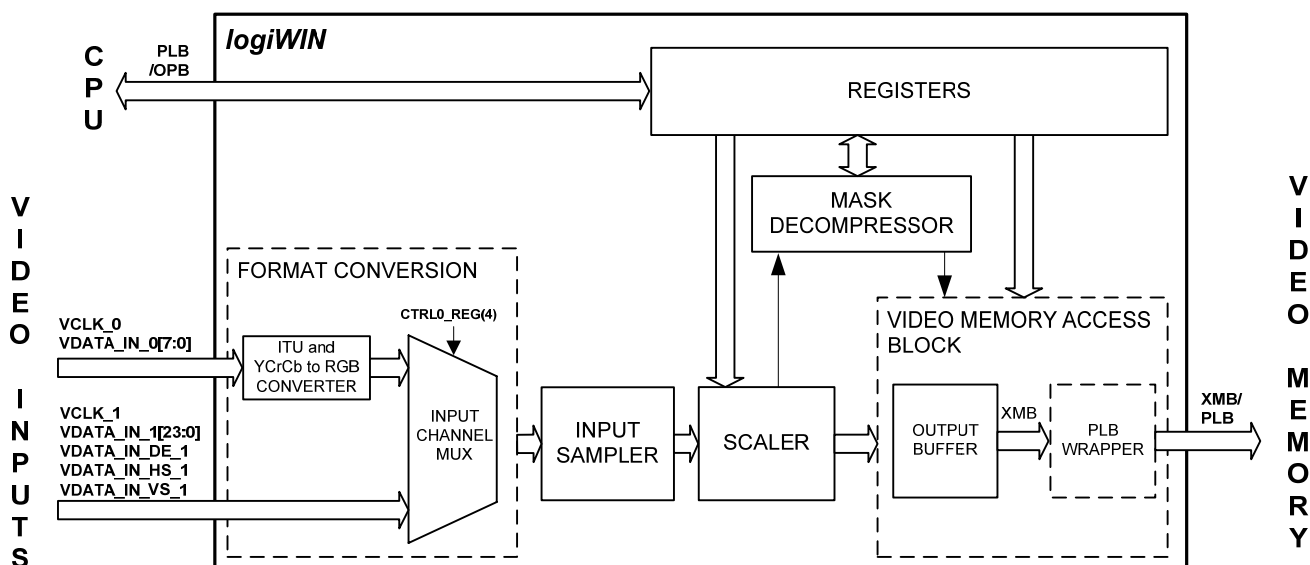


Figure 1: logiWIN Architecture

Features (cont)

- Free EDK reference design including the demo software application
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Simple Plug'n'play with other Xylon logicBRICKS™ IP cores, such as:
 - logiMEM Flexible Memory Controller
 - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
 - logiBMP Bitmap 2.5D Graphics Accelerator
 - logiCVC-ML Compact Multilayer Video Controller

Applications

- Car Infotainment and Telematics
- AutoPCs, Hand-held PCs
- Personal Digital Assistants
- SetTop Boxes, Video Phones
- Electronic Gadgets, etc.

General Description

The logiWIN is a frame grabber IP core from the Xylon logicBRICKS IP core library. It is designed to capture video input stream and give an output video formatted in variety of digital video formats. Its functions include scaling, cropping, positioning and masking the output image by non-rectangular masks. Interlaced input PAL/NTSC video streams can be deinterlaced. The interface to the frame buffer, or the video memory, is designed for SDRAM (SDR or DDR) or SRAM implementation. For easier system integration, the logiWIN uses CoreConnect PLB and OPB buses, as well as versatile choice of supported memory interfaces.

Functional Description

The Figure 1 presents internal logiWIN architecture. The logiWIN functional blocks are: Video Input Multiplexer and Formatting Block, Input Sampler, Scaler with Cropping Block, Mask Decompressor, Output Buffer (Memory Address Generator, PLBV46 Interface, Double / Triple buffering), PLB Wrapper and logiWIN Registers.

Video Input Multiplexer and Formatting Block

Instantiations of the Video Input Multiplexer and the ITU-to-RGB Converter depend on a number of input channels, nature of the input video stream, and the desired video output format.

Input Sampler

The input sampler module samples input video stream and transfers it into memory clock domain. This module does the input picture's cropping.

Scaler

The Scaler uses bilinear interpolation for scaling up and down input video's resolution. The input video can be zoomed in 64 times (scale up 64x), or zoomed out 16 times (scale down 1/16). This scaling range is quite wide, but there are some limitations related to the image quality.

Video resolution can be maximally scaled down two times without image quality losses. Further high-quality lossless scaling down is possible in the logiWIN cascade mode.

Mask Decompressor

The logiWIN can generate non-rectangle frames from output buffers by means of an optional compressed stencil programmed in the BRAM memory. The stencil's masking image is compressed by the Run-Length (RLE) encoding.

Output Buffer

The Output Buffer sub-block packs output data and bursts them towards external SDRAM or SRAM memories. It consists of three main parts: Memory Address Generator, Xylon Memory Bus (XMB) interface, and a part that handles double/triple buffering.

Memory Address Generator can be configured to store odd and even video picture lines to different or to the same memory addresses. The first lines storage method is suited for the "Wave" deinterlacing mode, while the second one better suits to the "Bob" deinterlacing. The "Bob" is default logiWIN deinterlacing mode.

The logiWIN controls multiple video buffers. The double or triple buffering prevents video flicker, shearing, and tearing artifacts.

PLB Wrapper

The CoreConnect PLB wrapper is an optional block enabling utilization of the PLBV46 bus as a memory interface instead of the XMB.

logiWIN Registers

The logiWIN's register interface can be configured as the CoreConnect OPB or PLB compatible interface.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with Xilinx Platform Studio. Many logiWIN configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiWIN VHDL configuration parameters

Parameter	Description
C_NUM_OF_INPUTS	Number of video inputs
C_INPUT_0_TYPE	Channel 1 video input type: ITU656 or RGB
C_INPUT_1_TYPE	Channel 2 video input type: ITU656 or RGB
C_ITU_TYPE	ITU video input type: ITU656 or ITU1120
C_ITU_BITS	Number of ITU bits. Valid values are 8 or 10
C_OUTPUT_TYPE	Video output type: YCbCr, RGB565, RGB888, ARGB6565, ARGB8888
C_USE_COLOR_MANAGEMENT	Includes or excludes color enhancement module
C_CONVERTER_USE_MULTIPLIER	Defines type of multipliers
C_CASCADE_ON	Enables cascaded scaling for lossless scale-down operations
C_USE_XSCALE	Horizontal scaling implementation on/off
C_USE_YSCALE	Vertical scaling implementation on/off

The logiWIN is designed with regard to adaptability to various cameras. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiWIN core or to supplement some of your specific functions, you can allow us to tailor the logiWIN to your requirements. The logiWIN behavioral model is available on request and at the extra cost.

Core I/O Signals

The core signals I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous set/reset
Memory Interface		
PLBV46 Master Interface	Bus	Refer to CoreConnect specification
XMB Interface	Bus	Xylon Memory Bus. Refer logiMEM specification
Register Interface		
PLBV46 Slave Interface	Bus	Refer to CoreConnect specification
OPB Slave Interface	Bus	Refer to CoreConnect specification
Video Input Signals		
VCLK_IN	Input	Video input clock used for both Channels if C_USE_EXT_CLOCKING = 1
VCLK_IN_SEL	Output	Video input clock select, ctrl_reg bit 4
VCLK_0	Input	Channel1 : Video input clock
VDATA_IN_0 (23:0)	Input	Channel1 : Video input data (for 8-bit ITU input type only 7:0 in use, for 10-bit ITU input type only 9:0 in use)
VDATA_IN_DE_0	Input	Channel1: Data enable (use only for RGB input type)
VDATA_IN_HS_0	Input	Channel1: Vsync (use only for RGB input type)

Signal	Signal Direction	Description
VDATA_IN_VS_0	Input	Channel1: Hsync (use only for RGB input type)
VCLK_1	Input	Channel2 : Video input clock
VDATA_IN_1 (23:0)	Input	Channel2 : Video input data (for 8-bit ITU input type only 7:0 in use, for 10-bit ITU input type only 9:0 in use)
VDATA_IN_DE_1	Input	Channel2: Data enable (use only for RGB input type)
VDATA_IN_HS_1	Input	Channel2: Vsync (use only for RGB input type)
VDATA_IN_VS_1	Input	Channel2: Hsync (use only for RGB input type)
Auxiliary Signals		
CURR_VBUFF(1:0)	Output	Triple buffering: Current video memory buffer
NEXT_VBUFF(1:0)	Input	Triple buffering: Next video memory buffer to write to
SW_VBUFF_REQ	Output	Triple buffering: Request for buffer switching
SW_VBUFF_GRANT	Input	Triple buffering: Buffer switching granted
INTERRUPT	Out	Interrupt signal, level sensitive, high active

Verification Methods

The logiWIN is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiWIN implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on different Xylon development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. The platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. Xylon's logiCRAFT platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

The logiCRAFT-CC Companion Chip Platform:

URL: <http://www.logicbricks.com/Products/logiCRAFT-CC.aspx>

The logiCRAFT6 Multimedia Evaluation/Development Platform:

URL: <http://www.logicbricks.com/Products/logiCRAFT6.aspx>

The logiTAP Platform for Embedded GUI Systems Developments:

URL: <http://www.logicbricks.com/Products/logiTAP.aspx>

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.02.	12.03.2009	Initial Xylon release – new doc template
2.03.	27.03.2009	Added VCLK_IN and VCLK_IN_SEL signals to the Table 3: Core I/O Signals
2.05.	15.03.2010	Updated Table 1 and Table 3
2.05.	06.04.2010	New doc template
2.06.	07.07.2010	Document name changed