

GENERAL

A simple SDRAM controller and its usage in logiCVC Reference Design are described. The Simple SDRAM controller is capable driving the 16-bit wide SDRAM using 3-clock CAS latency. Integral part of the Simple SDRAM controller is two-port SDRAM access arbiter. Through these two ports logiCVC and CPU access SDRAM contemporary. The SDRAM Controller accepts requests from logiCVC and CPU, managing priorities, granting access for these two units and generating address and control signals for SDRAM.

The Reference Design build of Simple SDRAM controller, logiCVC and CPU interface proves UMA (unified memory architecture) advantages in low cost systems. Beside Simple SDRAM controller the logiMEM – flexible multipart memory controller is available. logiMEM features Double or Single data Rate SDRAM control, multiport access arbiter, programmable arbitration schemas and others. For more information, please visit our WEB page at <http://www.logicbricks.com> or contact us at: info@logicbricks.com.

SDRAM Controller Architecture

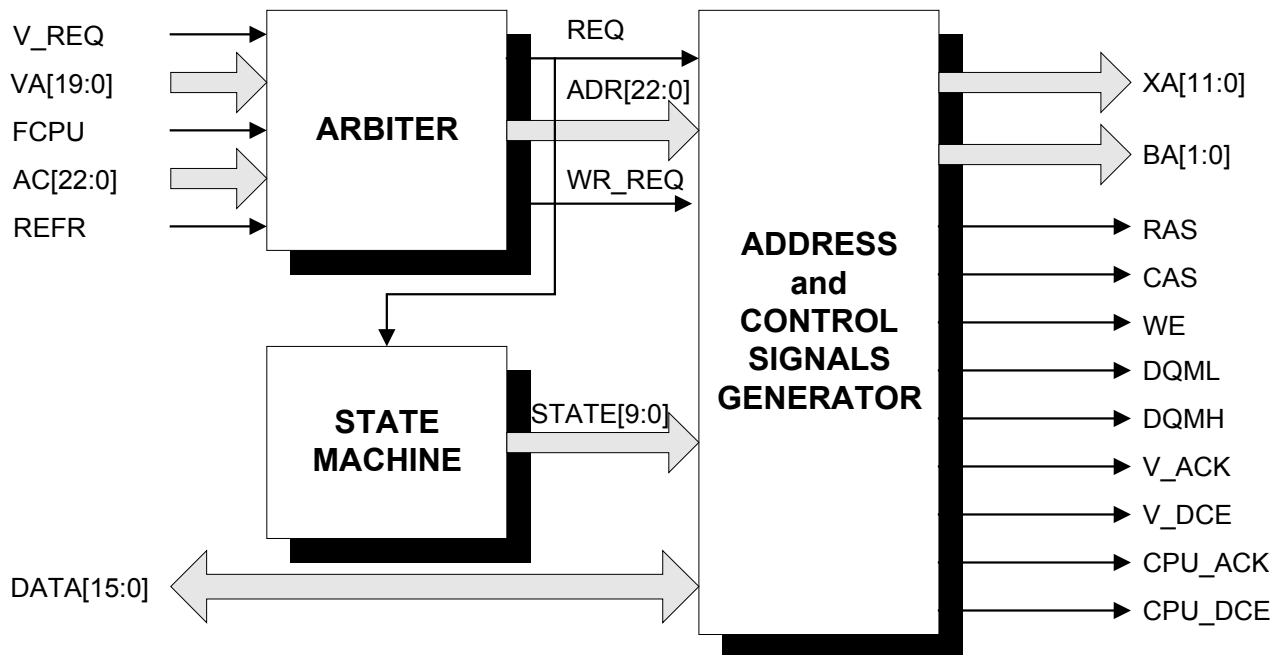


Figure1: SDRAM Controller Architecture

ARBITER

The Arbiter grants access to SDRAM to one of memory requesters: logiCVC, CPU and Memory Refresh requester. The arbiter grants accesses to SDRAM according to the assigned priorities. The logiCVC has highest priority, then the CPU, while the AUTO REFRESH has the lowest priority.

STATE MACHINE

The state machine controls the SDRAM access cycle. The state machine starts on the logiCVC, CPU or refresh SDRAM access requests. The state machine consists of nine states, each lasting one DCLK period. The state six (M6) is prolonged for the burst read cycles. The state machine waits in state nine (M9) if there are no active SDRAM access requests.

ADDRESS AND CONTROL SIGNAL GENERATOR

The Address and Control Signals Generator multiplexes and passes requesters addresses to the SDRAM address bus.

The SDRAM samples raw address (XA[11:0]) and bank address (BA[1:0]) when RAS is active, and column and bank address when CAS is active. The address generator issues SDRAM addresses on the SDRAM address bus at appropriate times.

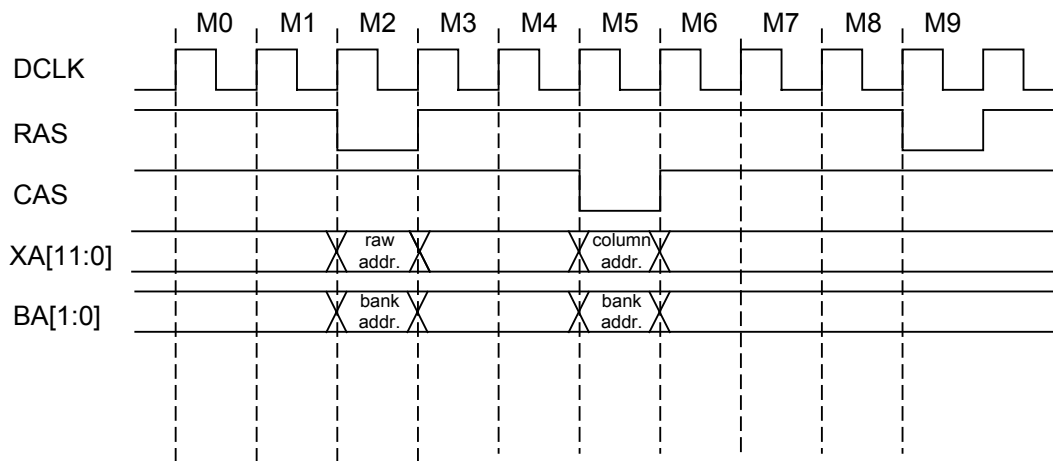


Figure2: Address Sampling

The Control Signal Generator drives acknowledges DCE signals for SDRAM requesters (the logiCVC and CPU) and generates RAS, CAS, WE, DQML and DQMH for SDRAM.

The Control Signal Generator drives acknowledge (x_ACK, V_ACK) signals to the granted access unit. When data are stable on the SDRAM data bus, the Control Signal Generator drives the DCE signal.

Depending upon the current state and operations that are to be accomplished, the Control Signal Generator generates the appropriate RAS, CAS and WE signal sequence, relative to the current SDRAM cycle type. All these signals are active low.

INITIALIZATION

Immediately after power-up (INIT_RST), SDRAM must be initialized. For 100µs the SDRAM controller must send an NOP command, followed by one precharge command, followed by a minimum of two auto refresh commands, and finally an MRS (memory register set) command. This procedure initializes the SDRAM.

LogiCVC access

The logiCVC must have the highest priority in order to preserve a continuous data flow between the video memory and the logiCVC Data FIFO. In order to efficiently use SDRAM bandwidth the data is read from SDRAM read data bursts. The SDRAM data bursts are written to Data FIFO.

The logiCVC requests memory every time that the Data FIFO is half-empty (V_REQ goes high). After the logiCVC receives memory access (V_ACK goes high), V_REQ goes to low and VA[19:0] increments.

The logiCVC reads data in burst read mode, 16 half-words long. The SDRAM is programmed to a maximum 8 word burst, by writing to the MRS register. The 16-bit word burst is accomplished as two 8-word consecutive bursts. After the first burst, the second block address is issued to SDRAM in a CAS cycle. The address generator generates a new column address. On the 16-bit data bus half-words come continuously, so the logiCVC sees it as one 16 half-words long burst.

Read access ends with PRECHARGE.

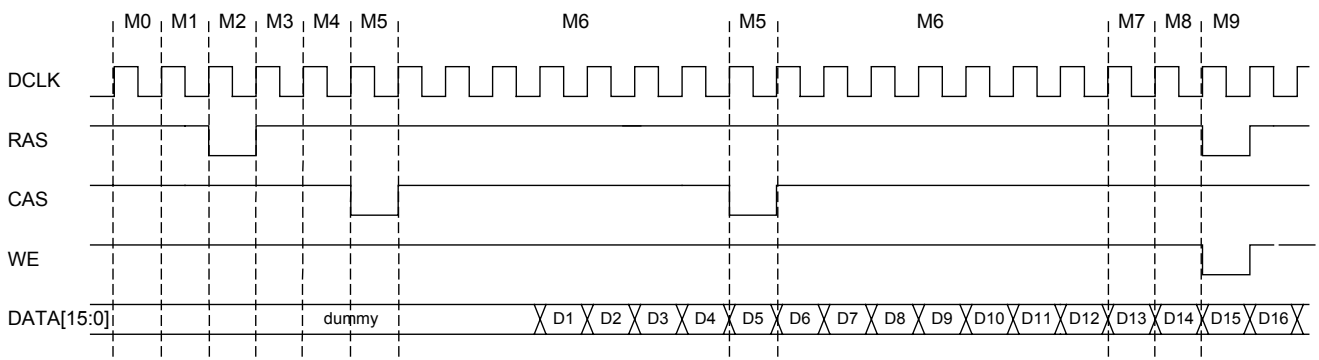


Figure3: Read Access of the logiCVC

The SDRAM data (DXR[15:0]) are captured in SDRAM on the rising edge of DCLK.

CPU access

The CPU has a lower access priority than the logiCVC. The CPU is capable of both reading and writing to SDRAM. As a difference to logiCVC the CPU access to SDRAM only as single byte. The arbiter generates signal (WR_REQ) that indicates read or write cycles to SDRAM control signals

The CPU reads and writes data in a single read and write cycle (burst=1), so every state lasts one DCLK period. The CPU reads and writes only one byte at a time. The data interface is 16-bits wide. The SDRAM controller drives DQML to high if an address is even and DQMH to high if an address is odd. DQML masks low and DQMH masks high bytes of data. The 8-bit wide data bus from the CPU must be connected to the both low and high byte on 16-bit wide SDRAM data bus.

The CPU read and write accesses ends with PRECHARGE.

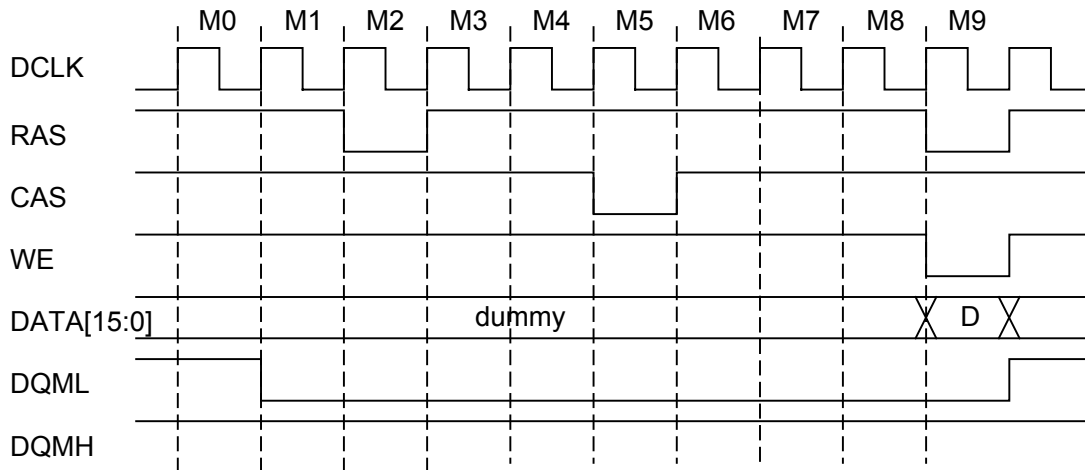


Figure4: CPU read access from even addresses

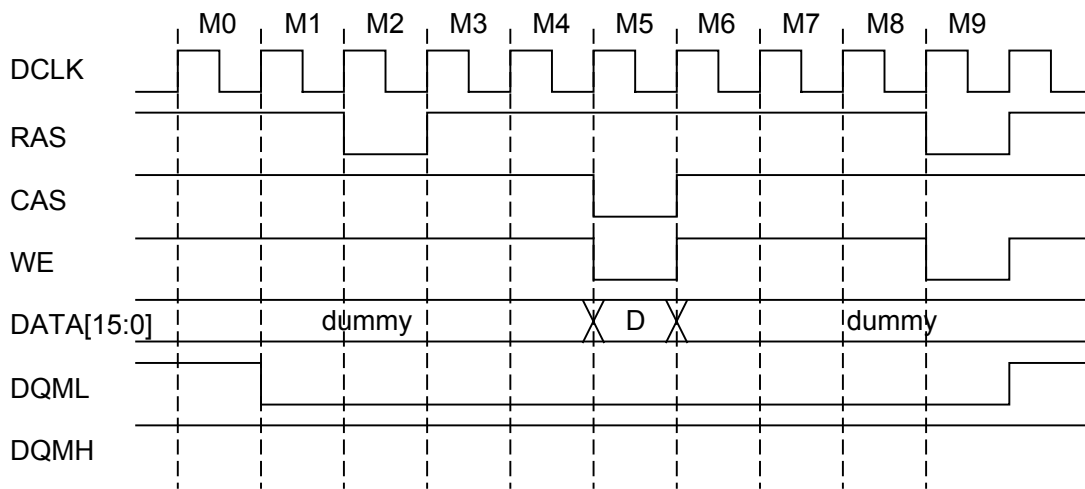


Figure5: CPU write access to even addresses

AUTO REFRESH

The SDRAM must be refreshed every 15,625 μ s (maximum) by issuing an AUTO REFRESH command. The timer generates the refresh request every 12288 (DCLK) clock cycles. The Refresh request has the lowest SDRAM access priority. The DLK period is 10ns, so approximately 12,288 μ s between each AUTO REFRESH cycle.