SUMMARY

Unified Memory Architecture (UMA) is shared memory between two or more devices. This architecture is an optimal solution for systems where memory bandwidth is sufficient to be shared among access devices. The logiCVC (Compact Video Controller) is aimed at low cost systems and can easily be implemented into UMA architecture systems.

INTRODUCTION

The UMA concept has been known for decades in computer industries. It can be found on the market from the low-cost PCs to Silicon Graphic Work Stations.

All video subsystems contain display memory (i.e., frame buffer) where display pixels are stored. During image preparation several elaborations of the pixels are performed. Finally, the prepared image is read from the frame buffer and transferred to the display. Due to standing requests for bigger, larger color depth and higher image refresh rate displays, the dedicated frame buffer concept has prevailed in the market. The dedicated frame buffer is physically separated from main memory in the dedicated frame buffer concept.

Contrary to this frame buffer memory organization concept, in UMA architecture frame the buffer is at the main, i.e., system memory. Dedicated frame buffers have evolved, due to the simple fact that video subsystem is huge consumers of memory bandwidth. In UMA architecture the CPU and video controller compete for memory access. If the video access is intense the CPU must wait, which decrease CPU performance.

The UMA system advantage is the flexible attribution of video buffer to existing system memory. The video buffer start address and size can easily be adjusted. Besides, UMA video systems have lower costs than dedicated video buffer solutions due to lack of an addition video memory chip.

The main logiCVC task is continuous refresh of the video page with specified refresh frame rates. The display refresh is a process of reading pixels from the frame buffer and sending them to the video display. The memory bandwidth is in direct proportion to the display resolution and display refresh rate. The critical issue in UMA architecture is memory bandwidth. For example, doubling the horizontal and vertical display resolution requires a fourfold increase in memory bandwidth. Increasing the color depth from 8 bpp (bits per pixel) to 16 bpp requires doubling the bandwidth. True color (color depth of 24 bpp) triples memory bandwidth.

The following table describes the cases mentioned above. The common display resolution and display color depths are given. The constant display refresh rate of 60Hz is chosen.

Resolution (pixels)	Color depth (bpp)	Used bandwidth (Mbytes/sec)
320 x 240	8	3.8
320 x 240	16	7.6
640 x 480	8	18.4
640 x 480	16	36.8
800 x 600	8	24
800 x 600	16	48
1024 x 768	8	39.3
1024 x 768	16	78.6

The logiCVC is working with 8bpp, and therefore keeps the required memory bandwidth at a low level. Note that 16 bpp is available for TFT only and the required memory bandwidth doubles.

The UMA eases CPU access to video (frame) memory buffer. As the frame buffer is in common system memory, the CPU can access it directly. On the contrary, in dedicated video buffer systems the CPU must access video memory through video controller logic. Also, in UMA systems the CPU doesn't need to copy display image data over a system bus.

UMA can be implemented with fewer memory chips, so the PCB can be smaller. All this lowers system cost, which is significant in embedded and low-cost systems.

The UMA does have some drawbacks. The UMA decreases overall system performance. The UMA is efficient for low resolution and low color depth video subsystems. By increasing the resolution refresh rate and color depth, video subsystem consume available memory bandwidth so the CPU and other memory access devices are slowed down.

REFERENCE DESIGN

Besides logiCVC, an logiCRAFT02 evaluation system and Reference design is available. For further information about the logicBRICKS™ products, please visit our WEB site.

A simplified reference design is given on figure 1. The SDRAM module indicates a Synchronous DRAM controller. All accesses to SDRAM memory go through an SDRAM controller.

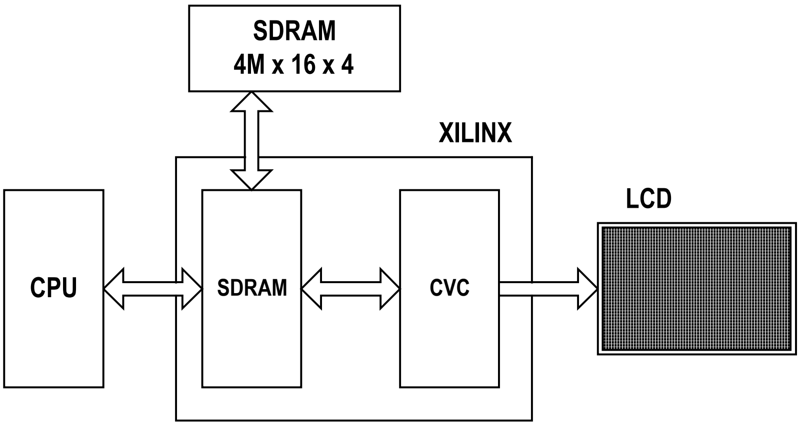

*Figure 1: S*implified reference design

The logiCVC shares common system memory with a CPU. The memory access arbiter assigns access rights to logiCVC or the CPU. The access arbiter is a part of the SDRAM controller. The SDRAM implemented in reference design features only three access ports. For further information about the memory controller check our logiMEM IP core.

Access to SDRAM is synchronous with a 100MHz clock. The Video buffer has a length of 1Mbyte.

Synchronous DRAM (SDRAM) is a good choice for UMA. In respect to older DRAMs or SRAMs, SDRAM has fast column access mode, i.e. burst mode. Inside a 512-wordss boundary access to data can be done once every clock rising edge. So the burst read or write speed is 100Mwords/sec.

Burst access is suitable for video frame buffer implementation; due the fact that during a display image refresh operation pixels are read sequentially. Also, CPU pixel elaboration during image creation usually accesses memory in a sequential way (polygon fill, horizontal lines).

Following two examples shows required memory bandwidth for two display types: TFT 800x600 and TFT 640x480. Calculated data can serve as evaluation of UMA systems where logiCVC and CPU interfaces share a memory bus.

It should be taken in consideration that system performance is improved if the CPU used in UMA systems has an internal cache. logiCVC internal FIFOs improve system performance as well.

For the memory bandwidth calculation, a 32-word depth FIFO in logiCVC is important. Half of FIFO is loaded in one memory access. The memory access depends on the SDRAM clock, memory latency and SDRAM controller implementation.

If we calculate the ideal memory bandwidth of a 100MHz SDRAM clock, it is 200Mbyte/s. The ideal memory bandwidth cannot be reached due to the memory refresh cycles and other SDRAM command cycles.

The pixel clock data rate is used in the memory bandwidth calculation. The pixel clock data rate is the rate by which the data are written to the display. For example, TFT with 800*600 resolution and a 32-pixel clock must be fed with data at a data rate of 32Mbyte/s.

The color depth is 8-bits per pixel. The ideal ratio between TFT memory bandwidth and SDRAM bandwidth will be:

32Mbyte/200Mbyte *100= 16%

In the ideal theoretic case, the TFT display occupies only 16% of the SDRAM memory bandwidth. The results in actual cases are slightly worse than the theoretical results. The time necessary for the display to empty half of the SDRAM FIFO can be calculated:

32bytes (half FIFO) * 1/32MHz (display pixel clock and 8-bit color depth) = 32 * 31ns approx. 1us

In the Reference design, FIFO loading access lasts 23 100MHz SDRAM clock periods. Besides 16 clock periods for accessing 16 words from memory, 7 clock periods are used for issuing commands to memory. The time for loading half of FIFO is:

23 x 10ns=230ns.

So the memory bandwidth occupied by TFT display as calculated in a real environment is:

230ns/1us * 100 = 23 %

The result is slightly better and depends on the quantity of dummy pixel periods, during which logiCVC doesn't access data from memory. The same calculation for a 640x480 resolution, 24Mhz pixel clock TFT display shows 17.25% of memory bandwidth required for display image refresh.

CONCLUSION

For low-cost systems UMA architecture is the best solution. The logiCVC can be implemented easily in UMA systems, which assures a quality video subsystem with modest memory bandwidth requirements.

The logiCVC is has been successfully implemented in industrial Human-Machine Interface (HMI) hardware platforms. The logiCVC is supported by WindowsCE and Linux operating systems.

The system contains a main CPU, NEC VR4300 microprocessor running internally at 166 MHz, with an external bus running at 50MHz. The FPGA provides a UMA SDRAM controller. Besides a NEC CPU and logiCVC, Fast DMA UART and IMAPCM Audio codes access the SDRAM.

Additional logicBRICKS™ cores provide full HMI, such as a Touch Panel and Keyboard controller. The described system is an example of a successful implementation of UMA using logiCVC. The device has been proved in the marketplace and it is one of the top performance WindowsCE devices in its market category.

