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Features

- Supports Spartan-3™, Spartan-3E™, Virtex-II Pro™, and Virtex-4™ Xilinx FPGAs
- Available under terms of the SignOnce IP License
- Supported 16 different ROP2 operations
- Contiguous and Array image addressing modes
- Color keyed transparency
- Color Expansion for Font acceleration
- Pattern BITBLT
- Support positive or negative Move operations without picture artefacts due to overlapping of unprocessed parts of the old picture
- Solid fill with any color
- Supported image formats: RGB8, RGBA8, RGB16, RGBA16, RGB24, and RGBA24
- Control of Pixel Alpha blending factors
- Porter&Duff compositing rules module
- Configurable CLB or BRAM FIFOs
- Configurable for Little or Big Endianess
- OPB bus CPU, and PLB bus (Video) memory interface
- Free EDK reference design including demo software application
- Parametrizable VHDL design that allows that allows tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK

Core Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	User's Guide Application Notes
Design File Formats	Encrypted VHDL VHDL sources available at extra cost
Constraint Files	logiBitBlt.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	Reference EDK design logiCRAFT2 demo application
Additional Items	HW platform logiCRAFT2 SW drivers for 3 rd party graphic libraries
Simulation Tool Used	
ModelSim	
Support	
Support provided by Xylon	

- Additional options:
 - logiMEM Flexible memory controller
 - logiCVC-ML Compact Multilayer Video Controller
 - logiWIN Versatile Video input

Application

- Car Infotainment and Telematics, AutoPCs, Personal Digital Assistants, Hand-Held PCs, SetTop Boxes, Video Phones, Electronic Gadgets

Table 1: Core Implementation Data³

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT/DSP48	DCM	MGT	PPC	Design Tools
Spartan-3™	XC3S1000-5	93	1768	298	2	8	0	0	N/A	N/A	ISE 8.1.03i
Spartan-3E™	XC3ES1200-5	76	1733	298	2	8	0	0	N/A	N/A	ISE 8.1.03i
Virtex-II Pro™	XC2VP4-7	105	1720	298	2	8	0	0	0	0	ISE 8.1.03i
Virtex-4™	XC4VFX12-12	146	1863	298	2	8	0	0	N/A	0	ISE 8.1.03i

*¹ – Assuming 8-bit and 16-bit pixel, 64-bit PLB and 32-bit OPB bus

*² – Assuming all core I/Os are routed off-chip, including full OPB and PLB interfaces

*³ – The slice consumption is lower in real designs due to optimizations on the PLB and the OPB busses

General Description

The logiBITBLT is a BITBLT IP core (BITBLT stands for Bit Block Transfer) that transfers a block of data from one (source) to another (destination) memory region. It mainly copies Bitmaps to/from the on-screen or off-screen video memory. The logiBITBLT can perform logical operations during this data transfer. Resulting Bitmap is created as a combination of a content of source memory region, a content of the destination memory region, and some pattern data.

The logiBITBLT significantly increases performance of the most common graphic (GUI) operations, and at the same time frees the CPU for other system tasks.

The logiBITBLT is designed for integration with Xylon's logiCVC-ML (Compact Multilayer Video Controller), logiWIN Versatile Video Input, and the logiMEM (SDR/DDR Memory controller). It can be also easily integrated into other, third-party designed SoC systems.

This IP is especially efficient in UMA (Unified Memory Architecture) designs.

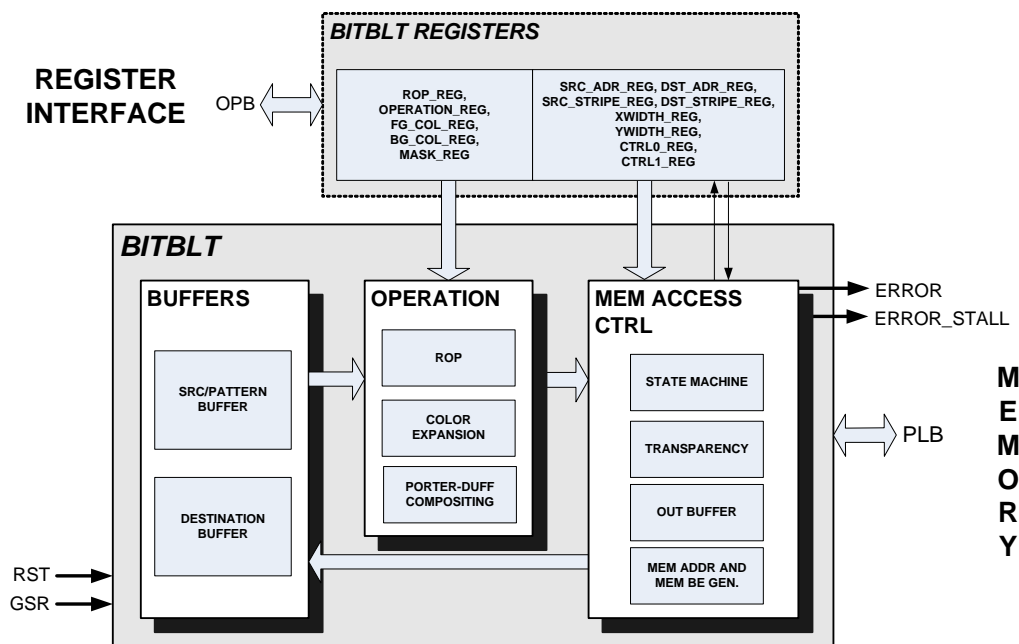


Figure 1: logiBITBLT Block Diagram

Pinout

The core signal names are shown in Figure 1 and described in Table 2.

Table 2: Core signal Pinout

Signal	Direction	Description
Global signals		
GSR	in	Global asynchronous set/reset (Xilinx)
RST	in	Global synchronous set/reset
Memory interface		
PLB bus	in/out	PLB bus for read/write into memory
Registers and control signals		
OPB bus	in/out	OPB bus for writing into configuration registers and communication between CPU and logiBITBLT
ERROR	out	Set for memory address overflow
ERROR_STALL	out	Set if logiBitBlt does not get access to memory in predefined period of time

Functional Description

The logiBITBLT core consists of: Memory Access Control Block, Buffers Block, BITBLT Operation Block and Optional Decompressors (Huffman, RLE) Block. The internal structure is shown in the Figure 1 block diagram.

Memory Access Control Block

The Memory Access Control Block is built of 4 sub-modules: Memory Address Generator, Memory Handshake Logic and Transparency, Output Buffer and State Machine. The block interfaces memory through Peripheral Local Bus (PLB). Control signals and data are handled accordingly to the PLB protocol.

The Memory Address Generator sets the memory address prior to reading or writing memory data. The address is generated accordingly to a stride length value, linear or continuous bitmap storage method, color expansion, or reach of width/high bitmap values during BITBLT operation. The Memory Handshake Logic requests video memory access, supervises write operations to the Output Buffer, and write of processed data back to the memory. It also executes transparency operation by controlling byte enables. The Output Buffer optimizes and increases the utilization of a memory bandwidth. The State Machine has control over accesses to source and destination memories.

Buffers

The bitmap data is stored to the Source or Destination Buffers. These FIFOs optimize and increase the utilization of a memory bandwidth, and can be implemented in CLB or BRAM Xilinx on-chip memory.

Operation

The BITBLT Operation Block controls a type of BITBLT operation. The following commands are available: Bitmap, Pattern or solid move/fill with ROP, with transparency or with color expansion. Some of these commands are contemporary available.

The Raster Operation Block performs logical operations between Source or Pattern, and the Destination Bitmap.

The Colour Expansion Block expands monochromatic bitmaps with a foreground and background color. Additionally it is used for Color solid fills and Color keyed transparency. The Porter&Duff Block executes compositing rules for combining of 2 images.

Core modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. A number of configuration parameters can be set up through the EDK GUI interface prior to the core's synthesis.

The logiBITBLT has been constructed with regard to adaptability to various display types and has been tested on several popular displays. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiBITBLT core, or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiBITBLT to your requirements.

The logiBITBLT source code (VHDL sources) is available at additional cost from Xylon.

Verification methods

The logiBITBLT is fully embedded into Xilinx Platform Studio and EDK tools. This tight integration with Xilinx integrated development environment tremendously shortens IP integration and verification time.

The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim.

The simulation and the implementation of the core do not require any particular skills beyond general Xilinx tools knowledge.

The logiBITBLT has been developed as part of a larger design. It has been tested in several designs and proved in large-scale production.

Recommended design experience

The users should have an experience in the following areas:

- ModelSim
- Xilinx ISE tools
- Xilinx Platform Studio (XPS) and the EDK
- Synchronous digital circuit design

Available Support Products

All logicBRICKS™ IP cores can be evaluated, tested and used on Xylon's logiCRAFT2 Multimedia and Infotainment Evaluation/Development platform.

The logiCRAFT2 is Spartan-3™ centric platform capable of driving up to three displays. The platform can simultaneously display different video streams on each screen.

Besides unique display driving capabilities, the logiCRAFT2 supports many networking types. The logiCRAFT2 is expandable and enables rapid hardware prototyping.

Detailed logiCRAFT2 info can be found at

http://www.logicbricks.com/html/evaluation_boards.htm.

Ordering Information

When inquiring please introduce following inquiring/order codes.

logiBITBLTnet	Virtex2, Virtex2Pro, Spartan2E and Virtex/Spartan2 netlist
logiBITBLTvhdl	VHDL source code

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact Xilinx sales office, or:

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