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Features

- Supports Spartan-3™, Spartan-3E™, Virtex-II Pro™, and Virtex-4™ Xilinx FPGAs
- Available under terms of the SignOnce IP License
- Supports LCD and CRT displays (easily tailored for special display types)
- 128x64 to 1024x768 display resolutions, and up to 16M colors
- Higher resolutions support available on request
- Supports up to 5 layers; the last one configurable as a background color
- Configurable layers' size and position
- Alpha blending and Color keyed transparency
- Pixel, Layer, or Color lookup table (CLUT) alpha blending mode can be set for each layer independently
- Packed pixel layer memory organization – pixel color depth 8-bpp (Color look up table), 16bpp Hicolor RGB 5-6-5 and Truecolor 24bpp
- Configurable PLB memory interface data width, 32 or 64 bits
- Programmable layer memory base address and stride
- Simple programming due to small number of control registers
- Programmable display data bus: 16-bit, 18-bit or 24-bit
- HW cursors
- Supports Digital Video (ITU-656: PAL and NTSC)
- Versatile and programmable sync signals timing
- Single clock input for all displays
- Tested with many popular displays
- Display power-on sequencing control signals

Core Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	User's Guide Application Notes
Design File Formats	Encrypted VHDL VHDL sources available at extra cost
Constraint Files	logiCVC.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	Reference EDK design logiCRAFT2 demo application
Additional Items	HW platform logiCRAFT2 SW drivers for 3rd party graphic libraries
Simulation Tool Used	
ModelSim	
Support	
Support provided by Xylon	

- Free EDK reference design including demo software application
- Parametrizable VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK
- Additional options:
  - logiMEM – Flexible memory controller
  - logiBITBLT – BITMAP graphic accelerator
  - logiWIN – Versatile Video input

Application

- Car Infotainment and Telematics, AutoPCs, Personal Digital Assistants, Hand-Held PCs, SetTop Boxes, Video Phones, Electronic Gadgets

Table 1: Core Implementation Data[3]

Family	Example Device	Fmax (MHz)	Slices[2]	IOB[1]	GCLK	BRAM	MULT/ DSP48	DCM	MGT	PPC	Design Tools
Spartan-3™	XC3S1000-5	54	1117	244	3	2	3	0	N/A	N/A	ISE 8.1.03i
Spartan-3E™	XC3ES1200-5	62	1239	244	3	2	3	0	N/A	N/A	ISE 8.1.03i
Virtex-II Pro™	XC2VP4-7	93	1015	244	3	2	3	0	0	0	ISE 8.1.03i
Virtex-4™	XC4VFX12-12	108	1202	244	3	2	3	0	N/A	0	ISE 8.1.03i

*1 – Assuming all core I/Os are routed off-chip, including full OPB and PLB bus interfaces
*2 – Assuming 32-bit PLB and OPB, 32-memory data width, 2 layers with Layer Alpha blending, 16-bit video data width, and 64K colors TFT support only
*3 – The slice consumption is lower in real designs due to optimizations on the PLB and the OPB busses

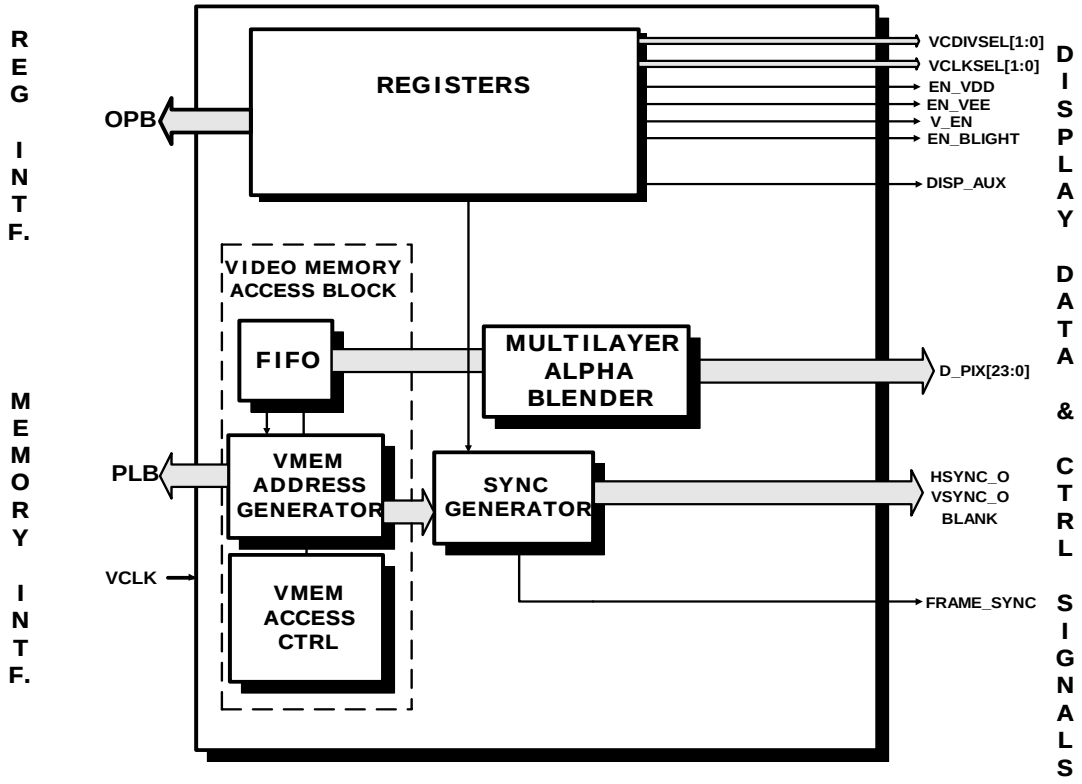

Figure 1: logiCVC-ML Block Diagram

General Description

The logiCVC-ML - Compact Multilayer Video Controller is a graphic video controller optimized for Xilinx FPGAs. It controls TFT flat panel displays and, by means of external video converters, S-Video, Composite Video devices and CRT displays (i.e. VGA monitors). A scaled-down logiCVC is available on request for non-TFT flat panel displays (TNM, STNM, etc.)

Multilayer support provides on screen display functions: alpha blending, color keyed transparency among layers, hardware cursors and fast scrolling and pan functions. All these features are supported in hardware and therefore require only low CPU processing power.

The interface to the frame buffer, or the video memory, is designed for SDRAM (SDR or DDR) or SRAM implementation. For easier system integration, logiCVC-ML uses Xilinx (IBM) CoreConnect PLB and OPB buses. The logiCVC-ML requires relatively low memory bandwidth and can be efficiently implemented in low-cost systems featuring Unified Memory Architecture (UMA).

Functional Description

The logiCVC-ML internal structure is shown on the block diagram on Figure 1.
The logiCVC-ML's funcional blocks are: Video Memory Access Block, Video Address Generator, FIFOs, Sync Generator, Multilayer Alpha Blender, Registers.

Video Memory Access Block

The Video Memory Access Block consists of 3 submodules: Video Memory Access Control, Video Memory Address Generator and FIFOs. The Video Memory Access Block fetches video data from the video memory over PLB to the local FIFOs. The Video Address Generator calculates video memory pointers for each layer. The Video Memory Access Block ensures that each FIFO is filled with the required amount of pixels and it performs arbitration between memory requests of each layer.
There is one FIFO per layer used for temporary storage of pixels. The FIFOs optimize the usage of video memory bandwidth and resynchronize incoming data to the display clock.

Sync Generator

The Sync Generator generates video synchronization signals. The duration of sync signals and their relative position to the display data (i.e., visible picture on the screen) can be adjusted through the set of logiCVC-ML registers.

Multilayer Alpha Blender

The Multilayer Alpha blender block consists of 5 equal configurable layer blocks. The outputs of the layer blocks are mixed according to alpha/transparent factors and layer priority. The Blender supports layer, pixel and color alpha blending methods.

Registers

All logiCVC-ML registers are instantiated in this block. The CPU has access to all these registers through an OPB (On-chip Peripheral Bus).

Core modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. The following logiCVC-ML configuration parameters are selectable prior to VHDL synthesis:

Table 2: logiCVC-ML VHDL configuration parameters

Description
PLB Bus configuration
OPB Bus configuration
logiCVC-ML registers OPB mem base address
Number of layers - 1,2,3,4,5
Layer color depth - 8,16,24,HW_Cursor mode: HW cursor (8-bpp mode) or 8-bpp, 16-bpp, 24bpp computer graphic or video input layer
Frame grabber streaming layer - None, 0, 1, 2, 3, 4 logiWIN Video input streaming to layer 0, 1, 2 , 3 or 4 or no Video input
Layer Alpha blending mode: layer, pixel, CLUT
Layer double buffer offset
Display data output – CMOS, LVDS

The logiCVC-ML has been constructed with regard to adaptability to various display types and has been tested on several popular displays (see Table 3). However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiCVC-ML core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiCVC-ML to your requirements. The logiCVC-ML source code (VHDL sources) is available at additional cost from Xylon.

Table 3: Partial list of displays tested with logiCVC-ML

Display	Producer	Resolution
LQ057Q3DC02	Sharp	320x240 Col TFT
LQ065T9DR51U	Sharp	400x240 Col TFT
LJ64H034	Sharp	640x400 Elumin.
NL6448AC33	NEC	640x480 Col TFT
LQ10D36	Sharp	640x480 Col TFT
TD070WGCB2	Toppoly	854x480 Col TFT
LQ121S1DG11	Sharp	800x600 Col TFT
LQ150X1DG11	Sharp	1024x768 Col TFT
Various proprietary automotive displays		800x480 TFT 400x234 TFT
CRT		640x480 / 800x600 VGA

Verification methods

The logiCVC-ML is fully embedded into Xilinx Platform Studio and EDK tools. This tight integration with Xilinx integrated development environment tremendously shortens IP integration and verification time.

The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim.

The simulation and the implementation of the core do not require any particular skills beyond general Xilinx tools knowledge.

The logiCVC-ML has been developed as part of a larger design. It has been tested in several designs and proved in large-scale production.

Available Support Products

All logicBRICKSTM IP cores can be evaluated, tested and used on Xylon's logiCRAFT2 Multimedia and Infotainment Evaluation/Development platform.
The logiCRAFT2 is Spartan-3TM centric platform capable of driving up to three displays. The platform can simultaneously display different video streams on each screen.
Besides unique display driving capabilities, the logiCRAFT2 supports many networking types. The logiCRAFT2 is expandable and enables rapid hardware prototyping.
Detailed logiCRAFT2 info can be found at http://www.logicbricks.com/html/evaluation_boards.htm.

Ordering Information

When inquiring, please use the following inquiry/order codes.

Table 4: logiCVC-ML ordering codes

logiCVC-MLeconf	Encrypted VHLD
logiCVC-MLvhdl	VHDL sources

Pinout

Signal names are shown in Figure 1 and described in Table 5.

Table 5: Core Signal Pinout

Video Memory bus		
Signal	**Type**	**Description**
PLB BUS	in/out	Video memory data, address, control
Display control signals		
HSYNC_O	out	Horizontal sync
VSYNC_O	out	Vertical sync
PIX_CLK	out	Pixel clock
BLANK	out	Blank/display enable at TFT
D_PIX[*VIDEO_DATA_WIDTH*-1:0]	out	Video pixel data bus
LVDS_CLK _pos/_neg	out	Alternative LVDS Clock
LVDS_D_PIX[3:0] _pos/_neg	out	Alternative LVDS Pixel data bus
Auxiliary signals		
VCLK	in	Video clock input
VCDIVSEL[1:0]	out	Video clock divider select
VCLKSEL[1:0]	out	Video clock select
EN_VDD	out	Enable Vdd power supply
EN_VEE	out	Enable Vee power supply
EN_BLIGHT	out	Enable backlight power supply
V_EN	out	Enable display control/data signals
CPU control signals		
OPB_BUS	in/out	Reg data, select, control

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact the Xilinx sales office, or:

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