

# logiMEM SDR/DDR SDRAM Memory Controller

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Product Specification



Designed by **XYLON**

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## Features

- Available under terms of the SignOnce IP License
- Supports Spartan™-3, Spartan-II, Virtex-II Pro™, Virtex™-II, Spartan-II-E, Virtex-E, and Virtex FPGAs
- Supports industry standard SDR and DDR SDRAM memory devices
- Supports Processor Local Bus (PLB) system interface
- Programmable system data interface speed (for DDR SDRAM only)
- Supports SDRAM data path widths of 8, 16, and 32 bits
- Little-endian connections to memory devices
- Programmable burst length that applies for both Read and Write cycles
- Supports overlapped read and write transfers
- Data masking Byte enable signals supported for Write cycles
- Programmable SDR/DDR SDRAM row and column address width
- Programmable number of SDR/DDR SDRAM chips
- Programmable SDR/DDR SDRAM timings (i.e. CAS latency)

**Table 1: Core Implementation Data**

Supported Family	Device Tested	CLB Slices <sup>2</sup>	Clock IOBs <sup>1</sup>	IOBs <sup>1</sup>	GCLK	Performance (MHz) <sup>3</sup>	Xilinx Tools
Spartan 3	XC3S1000	214	1	350	2	133	ISE7.1i

\*1 – Assuming all core I/Os are routed off chip  
\*2 – 16-bit DDRAM configuration with PLB interface  
\*3 – Depends on number of PLB masters

Core Facts	
<b>Core Specifics</b>	
See Table 1	
<b>Provided with Core</b>	
Documentation	User's Guide
Design File Formats	NGC netlist, VHDL sources
Constraint Files	logiMEM.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	Implementation examples
Additional Items	Synthesis scripts
<b>Simulation Tool Used</b>	
ModelSim	
<b>Support</b>	
Support provided by XYLON	

## Features (cont)

- Supported different SDR/DDR SDRAM initialization sequences
- Automatic refresh generation with programmable refresh intervals
- Supported memory Self-refresh mode
- Supported memory Power Down mode
- Low gate count, high speed, high performance solution
- Parametrizable VHDL design that allows customization and can be tailored to fulfill your needs
- Prepared for Xilinx Platform Studio (XPS) and the EDK

## Application

- Video systems and image processing
- Embedded computing
- Communication and Networking equipment
- High performance peripheral equipment

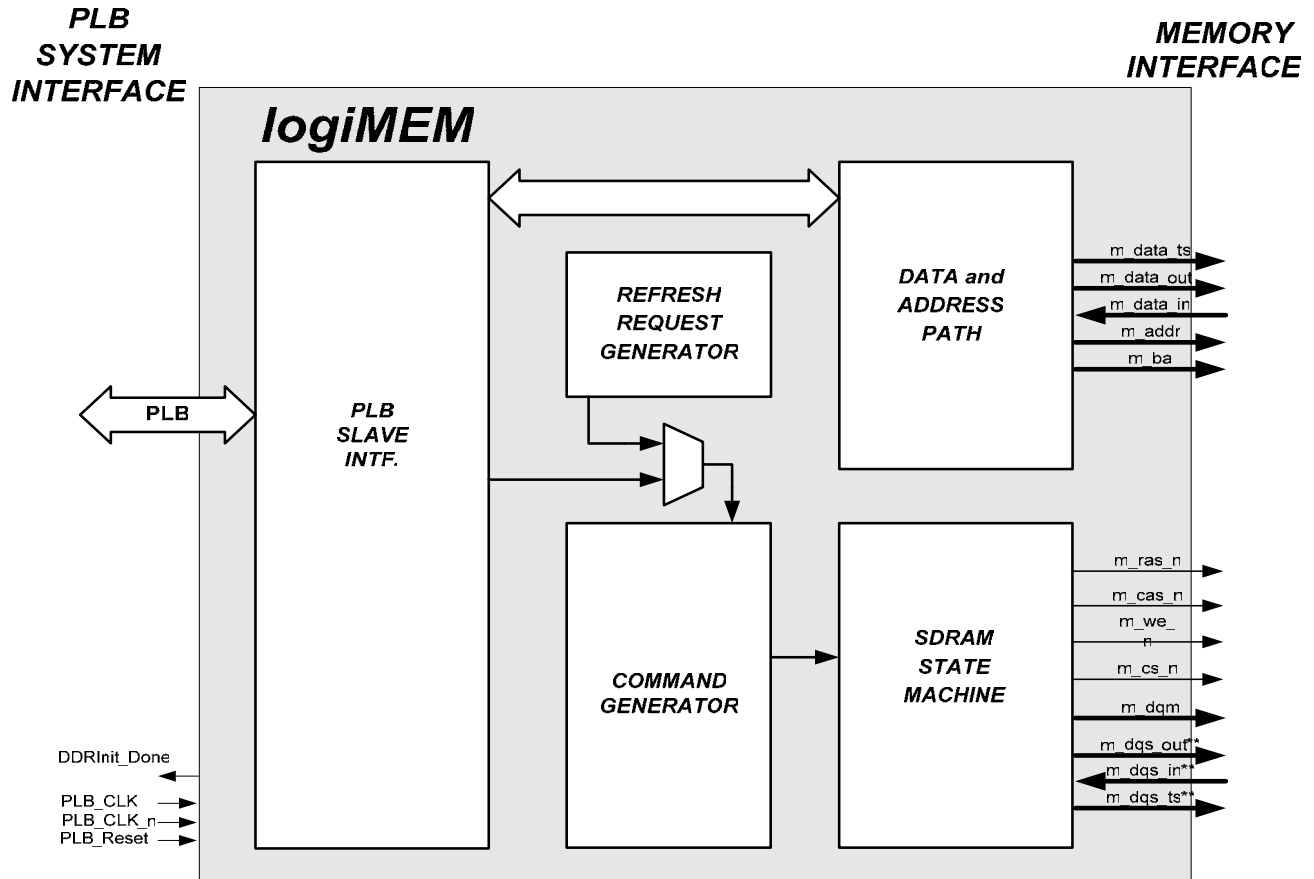


Figure 1: The logiMEM – block schematic

## General Description

The logiMEM SDR/DDR SDRAM controller provides a powerful, yet simple-to-use interface between the industry standard memory devices and several processor or DMA devices which share the same physical memory devices and access them through Processor Local Bus (PLB). Written in generic RTL VHDL, it is extremely adoptable and can fit into high-end SoRC (System on Reconfigurable Chip) systems, as well as into low-end systems featuring UMA (Unified Memory Architecture) system architecture.

Overall bandwidth performances are significantly improved by equally supported Burst Read and Burst Write memory access. Supported Self-refresh and Power Down memory modes are important for power saving applications.

The logiMEM is targeted towards modern Xilinx FPGA architectures. High controller's performances can be

obtained through an auto-place and an auto-route design flow; no hand floorplaning is required. Supplied constraint files control the final implementation result. In order to achieve portability of the core source code across various Xilinx FPGA families, all IO blocks, clock drivers, and family-specific circuits are implemented outside the core.

Using the logiMEM SDRAM controller is highly recommended in video applications where digital video, sourced from different sources, could be mixed inside the video frame buffer in an easy and natural manner.

## Functional Description

The logiMEM SDR/DDR SDRAM controller is partitioned into modules as shown in Figure 1 and described below.

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## Slave PLB Interface

The PLB Slave interface module assures bus control and correct logiMEM's attachment to the PLB, through shared, but decoupled, address, read data, and write data busses. Besides data busses, a plurality of transfer control and status signals for each data bus are also connected to, and controlled by this module.

## Command Generator

The Command Generator accepts commands decoded by the PLB Slave interface module (system interface), and generates corresponding commands for a memory interface.

## Data and Address Path

Data and Address Path module accepts the address and data from/to the PLB Slave interface module, converts them into the memory interface address and data format.

It must be noted that the IBM's CoreConnect bus uses bit and byte labelling accordingly to the big-endian format. Majority of SDR/DDR SDRAM chips regularly support the little-endian format.

The Data and Address path module takes care on endianness, and makes proper conversions.

## Refresh Request Generator

The Refresh Request Generator takes care of a proper time between the two refresh cycles. The refresh cycle period is defined prior to core synthesis.

## SDRAM State Machine

This block provides the appropriate timing and drive to the address and controls pins of the SDR/DDR SDRAM, according to the requested command.

## User-defined Parameters

The logiMEM controller can be customized for a particular system by defining a number of parameters at compile-time. These parameters are:

- C\_MEM0\_BASEADDR : base address
- C\_MEM0\_HIGHADDR : high address
- C\_PLB\_NUM\_MASTERS : number of PLB masters
- C\_PLB\_MID\_WIDTH : number of bits for encoding PLB
- C\_PLB\_AWIDTH : width of PLB addr bus
- C\_PLB\_DWIDTH : width of PLB data buses
- C\_PLB\_CLK\_PERIOD\_PS : PLB clock period (ps)
- C\_NUM\_CLK\_PAIRS : number of DDR clk pairs
- C\_NUM\_BANKS\_MEM : number of DDR mem banks
- C\_FAMILY : targeted FPGA family
- C\_DDR\_TMRD : delay Load Mode Register
- C\_DDR\_TWR : delay for write recovery
- C\_DDR\_TWTR : write-to read delay
- C\_DDR\_TRAS : Active to Precharge delay
- C\_DDR\_TRC : Active to Active/Refresh delay
- C\_DDR\_TRFC : delay after AutoRefresh
- C\_DDR\_TRCD : Active to Read/Write delay
- C\_DDR\_TRRD : Active to Active (another row) delay
- C\_DDR\_TRP : delay after Precharge
- C\_DDR\_TREFC : SDRAM Refresh interval
- C\_DDR\_TREFI : time of avg. periodic refresh
- C\_DDR\_CAS\_LAT : CAS latency
- C\_DDR\_DWIDTH : DDR data bus width
- C\_DDR\_AWIDTH : DDR address bus width
- C\_DDR\_COL\_AWIDTH : DDR column addr width
- C\_DDR\_BANK\_AWIDTH : DDR bank address width
- C\_SIM\_INIT\_TIME\_PS : DDR initialization time (for simulation only)

Table 1: Core Signal Pinout

	Signal name	Active	Dir.	Description
PLB System Interface Port <sup>1</sup>	PLB_ABus[0:C_PLB_AWIDTH-1]	na	in	PLB address bus
	PLB_PAVValid	high	in	PLB primary address valid indicator
	PLB_SAVValid	high	in	PLB secondary address valid indicator
	PLB_rdPrim	high	in	PLB secondary to primary read request indicator
	PLB_wrPrim	high	in	PLB secondary to primary write request indicator
	PLB_masterID[0:C_PLB_MID_WIDTH-1]	na	in	PLB current master identifier
	PLB_abort	high	in	PLB abort bus request indicator
	PLB_busLock	high	in	PLB bus lock
	PLB_RNW	na	in	PLB read not write
	PLB_BE[0:(C_PLB_DWIDTH/8)-1]	high	in	PLB byte enables
	PLB_MSize[0:1]	na	in	PLB master data bus size
	PLB_size[0:3]	na	in	PLB transfer size
	PLB_type[0:2]	na	in	PLB transfer type
	PLB_compress	high	in	PLB compressed data transfer indicator
	PLB_guarded	high	in	PLB guarded transfer indicator
	PLB_ordered	high	in	PLB synchronize transfer indicator
	PLB_lockErr	high	in	PLB lock error indicator
	PLB_wrDBus[0:C_PLB_DWIDTH-1]	na	in	PLB write data bus
	PLB_wrBurst	high	in	PLB burst write transfer indicator
	PLB_rdBurst	high	in	PLB burst read transfer indicator
	PLB_pendReq	high	in	PLB pending bus request indicator
	PLB_pendPri[0:1]	na	in	PLB pending request priority
	PLB_reqPri[0:1]	na	in	PLB current request priority
	SI_addrAck	high	out	logiMEM (Slave) address acknowledge
	SI_SSize[0:1]	na	out	logiMEM Slave data bus size
	SI_wait	high	out	logiMEM Slave wait indicator
	SI_rearbitrate	high	out	logiMEM Slave rearbitrate bus indicator
	SI_wrDAck	high	out	logiMEM Slave write data acknowledge
	SI_wrComp	high	out	logiMEMSlave write transfer complete indicator
	SI_wrBTerm	high	out	logiMEM Slave terminate write burst transfer
	SI_rdDBus[0:C_PLB_DWIDTH-1]	na	out	logiMEM Slave read data bus
	SI_rdWdAddr[0:3]	na	out	logiMEM Slave read word address
SI_rdDAck	high	out	logiMEM Slave read data acknowledge	

<sup>1</sup> PLB Slave interface – for detailed description, please check PLB bus specs.

	SI_rdComp	high	out	logiMEM Slave read transfer complete indicator
	SI_rdBTerm	high	out	logiMEM Slave terminate read burst transfer
	SI_MBusy[0:C_PLB_NUM_MASTERS-1]	na	out	logiMEM Slave busy indicator
	SI_MErr[0:C_PLB_NUM_MASTERS-1]	na	out	logiMEM Slave error indicator
<b>System signals</b>	PLB_clk	na	in	PLB bus clock and SDRAM logic clock
	Clk90_in	na	in	PLB bus clock phase shifted by 90 degrees
	PLB_Rst	high	in	PLB reset
<b>DDR SDRAM signals</b>	DDR_Clk[C_NUM_CLK_PAIRS-1:0]	na	out	SDRAM clock signal
	DDR_Clk_n[C_NUM_CLK_PAIRS-1:0]	na	out	SDRAM clock signal shifted by 180 degrees
	DDR_CKE[C_NUM_BANKS_MEM-1:0]	high	out	SDRAM clock enable
	DDR_CSn[C_NUM_BANKS_MEM-1:0]	low	out	SDRAM chip select signal
	DDR_RAS_n	low	out	SDRAM command input
	DDR_CAS_n	low	out	SDRAM command input
	DDR_WE_n	low	out	SDRAM command input
	DDR_DM[C_DDR_DWIDTH/8-1:0]	high	out	SDRAM data masks, mask individual bytes during data write
	DDR_BankAddr[C_DDR_BANK_AWIDTH-1:0]	na	out	SDRAM bank address
	DDR_Addr[C_DDR_AWIDTH-1:0]	na	out	Row/Column SDRAM address
	DDR_DQ_o[C_DDR_DWIDTH-1:0]	high	out	SDRAM data bus output
	DDR_DQ_i[C_DDR_DWIDTH-1:0]	na	in	SDRAM data bus input
	DDR_DQ_t[C_DDR_DWIDTH-1:0]	high	out	SDRAM data bus Three-State control
	DDR_DQS_i[C_DDR_DWIDTH/8-1:0]	na	in	SDRAM data strobe input
	DDR_DQS_o[C_DDR_DWIDTH/8-1:0]	high	out	SDRAM data strobe output
DDR_DQS_t[C_DDR_DWIDTH/8-1:0]	high	out	SDRAM data strobe Three-State control	

## Pinout

The pinout of the logiMEM SDR/DDR SDRAM Multi-port Controller is shown in Figure 1 and described in Table 1. It has not been fixed to specific FPGA I/O, allowing maximal flexibility during the core integration into user's system.

## Core Modifications

Source Code customizing is available through XYLON design services. Unfortunately, XYLON cannot provide support for user's Source Code modifications.

## Verification methods

The logiMEM IP core is instantiated into HDL test-bench as an UUT (Unit under test). The test-bench simulates all other required hardware modules: clock generation, a module requesting DMA accesses and whole memory subsystem (delivered by courtesy of Micron Inc.). The ViewSim and ModelSIM simulation tools are used.

## Recommended design experience

The users should have experience in the following areas:

- Synchronous digital circuit design
- Xilinx ISE tools
- Xilinx Platform Studio (XPS) and the EDK
- ModelSim

## Ordering Information

When inquiring, please use the following inquiry/order codes.

logiMEMvhd1	Core VHDL sources, Virtex-II/Virtex/Spartan-II netlist generated for three access ports and 8-bit SDRAM
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## Related Information

Micron Inc.

Micron Technology, Inc., is a Fortune 500 company and one of the world's leading manufacturers of superior-quality memory semiconductors.

For information about Micron DRAM Simulation models contact:

URL: [www.micron.com](http://www.micron.com)

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