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Features

- Supports Spartan-3™, Spartan-3E™, Virtex-II Pro™, and Virtex-4™ Xilinx FPGAs
- Available under terms of the SignOnce IP License
- Supports versatile digital video input formats:
 - ITU656 (PAL, NTSC)
 - VGA
- Built-in YUV to RGB converter
- Wide range of input and output resolutions from 64x64 to 2048x2048
- Video stream real-time scaling using LMS (Least Mean Square) algorithm:
 - Scale-up (zoom-in) up to 4 times
 - Scale-down (zoom-out) up to 2 times
- Wider scaling range possible by scaler cascading
- Picture cropping and positioning
- Configurable PLB bus for video memory interface
- Configurable OPB bus for CPU interface
- Free EDK reference design including demo software application
- Parametrizable VHDL design that allows tuning of slice consumption and features set

Core Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	User's Guide
Design File Formats	Encrypted VHDL, VHDL RTL sources available at extra cost
Constraint Files	logiWIN.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	Reference EDK design logiCRAFT2 demo application
Additional Items	Verification and Evaluation platform logiCRAFT2 Software drivers for 3 rd party graphic libraries
Simulation Tool Used	
ModelSim	
Support	
Support provided by Xylon	

- Additional options :
 - logiMEM – Flexible memory controller
 - logiBITBLT – BITMAP graphic accelerator
 - logiCVC-ML – Versatile Multilayer Video Controller
 - Image 90 degree rotation
 - LVDS or CVBS output encoders

Application

- Car Infotainment and Telematics, AutoPCs, Personal Digital Assistants, Hand-Held PCs, SetTop Boxes, Video Phones, Electronic Gadgets

Table 1: Core Implementation Data⁴

Family	Example Device	Fmax (MHz)	Slices ²	IOB ¹	GCLK	BRAM	MULT/DSP48 ³	DCM	MGT	PPC	Design Tools
Spartan-3™	XC3S1000-5	75	1202	222	3	5	0	0	N/A	N/A	ISE 8.1.03i
Spartan-3E™	XC3ES1200-5	86	1196	222	3	5	0	0	N/A	N/A	ISE 8.1.03i
Virtex-II Pro™	XC2VP4-7	97	1082	222	3	5	0	0	0	0	ISE 8.1.03i
Virtex-4™	XC4VFX12-12	139	982	222	3	5	0	0	N/A	0	ISE 8.1.03i

^{*1} – Assuming all core I/Os are routed off-chip

^{*2} – Assuming configuration with ITU656 decoder, YCrCb2RGB converter, de-interlacer, 64-bit PLB and 32-bit OPB interfaces, 24-bit pixel

^{*3} – The usage of Xilinx hard-core multipliers is controlled by VHDL generic. The example configuration does not use hard-core multipliers

^{*4} – The slice consumption is lower in real designs due to optimizations on the PLB and the OPB busses

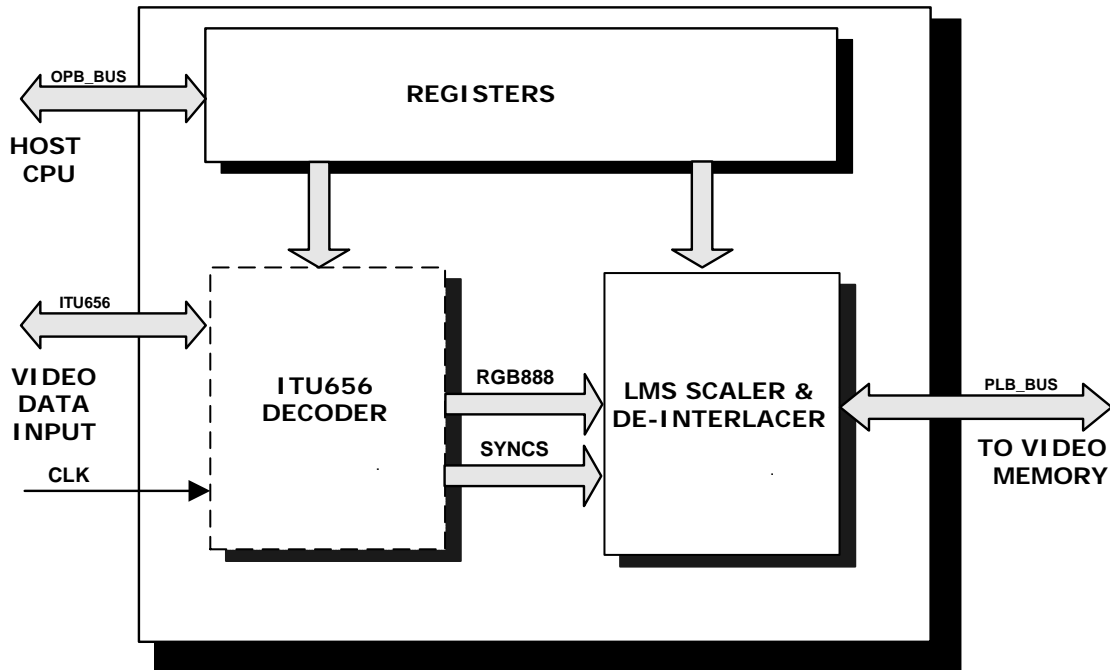


Figure 1: logiWIN Block Diagram

General Description

The logiWIN is a picture process unit. It accepts versatile digital video input streams, converts them to RGB format and adapts the picture to the targeted video format.

For ITU656 input video stream, there is an integrated ITU656 decoder and YUV to RGB converter. The logiWIN supports picture scaling, cropping and positioning on real-time video.

There is an optional built-in deinterlacer for interlaced input video streams. The LMS (Least Mean Square) anti-

aliasing algorithm, used for scaling, guarantees high picture quality without visible artifacts.

The processed picture is stored to the video memory using the PLB interface. All required parameters can be easily programmed through a set of registers accessible through OPB CPU interface.

The parametrizable VHDL design allows customization.

Functional Description

The logiWIN internal structure is shown on the block diagram on Figure 1.

The logiWIN's functional blocks are: Format Converter, Buffers, Resize Unit, Memory Access Controller and Registers.

Format Converter

The Format Converter accepts various video input formats and adapts them to output RGB format. Optionally, it contains an ITU656 decoder, YUV to RGB converter or color depth converter. If more than one video input is in use, video multiplexer is instantiated.

Buffers

The LMS scaling algorithm requires two lines from the input picture accessible at the same time. The block "Buffers" contains memory for temporary storage of these two lines.

Memory Access Control

The memory access control block buffers the processed video stream and transfers the data over PLB to video memory. This block also performs cropping and positioning. In this way, the video can be reduced in size, which reduces bandwidth requirements, and positioned at the required memory location.

Registers

The logiWIN registers can be accessed through an OPB data bus. Each of the above-mentioned functional blocks is configured with its corresponding register.

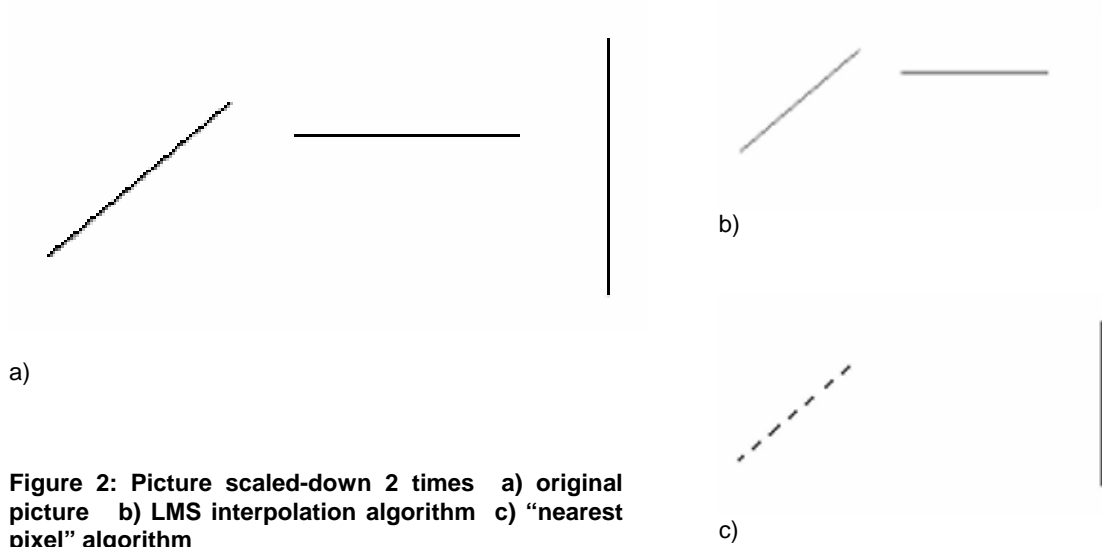


Figure 2: Picture scaled-down 2 times a) original picture b) LMS interpolation algorithm c) "nearest pixel" algorithm

Pinout

The core signal names are shown in Figure 1 and described in Table 2.

Table 2: Core signal Pinout

Signal	Direction	Description
CPU Interface		
OPB bus	in/out	OPB bus signals
Memory Interface		
PLB bus	in/out	PLB bus signals
ITU656		
ITU656[7:0]	in	ITU656 stream signals
VGA		
RGB[23:0]	in	RGB data signals
PIX_CLK	in	VGA pixel clock
HSYNC(ALIGN)	in	HSYNC aligned on VGA pixel clock
HSYNC(CABLE)	in	HSYNC signal from VGA cable
VSYNC(CABLE)	in	VSYNC signal from VGA cable

Core modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. A number of configuration parameters are selectable prior to VHDL synthesis.

The logiWIN has been constructed with regard to adaptability to various video input types and has been tested on several graphic embedded systems. However, there may be instances where source code modification is necessary.

Therefore, if you wish to reach the optimal use of the logiWIN core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiWIN to your requirements.

The logiWIN source code (VHDL sources) is available at additional cost from Xylon.

Verification methods

The logiWIN is fully embedded into Xilinx Platform Studio and EDK tools. This tight integration with Xilinx integrated development environment tremendously shortens IP integration and verification time.

The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim.

The simulation and the implementation of the core do not require any particular skills beyond general Xilinx tools knowledge.

The logiWIN has been developed as part of a larger design. It has been tested in several designs and proved in large-scale production.

Available Support Products

All logicBRICKS™ IP cores can be evaluated, tested and used on Xylon's logiCRAFT2 Multimedia and Infotainment Evaluation/Development platform.

The logiCRAFT2 is Spartan-3™ centric platform capable of driving up to three displays. The platform can simultaneously display different video streams on each screen.

Besides unique display driving capabilities, the logiCRAFT2 supports many networking types. The logiCRAFT2 is expandable and enables rapid hardware prototyping.

Detailed logiCRAFT2 info can be found at http://www.logicbricks.com/html/evaluation_boards.htm.

Ordering Information

When inquiring please use the following inquiring/order codes.

Table 3: logiWIN ordering codes

logiWINeconf	Encrypted VHDL
logiWINvhdl	VHDL source code

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Recommended design experience

Users should have experience in the following areas:

- Synchronous digital circuit design
- Xilinx ISE tools
- Xilinx Platform Studio (XPS) and the EDK
- ModelSim

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact Xilinx sales office, or:

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