



logiCVC Compact Video Controller

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Product Specification



Designed by **XYLON**

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Features

- Available under terms of the SignOnce IP License
- Supports Virtex™-II, Virtex™, Spartan™-II, Spartan™-3, Spartan™-3E, and Virtex™-4 FPGAs
- 128x64 to 1024x768 display resolution and up to 64K colors (16bpp)
- Support for single and double panel displays
- Gray and color shades using XCOLOR™; up to 8 gray levels or 256 colors for STN displays
- Programmable display data bus: 1, 2, 4, 8 or 16-bits
- Supports Electroluminescent, Plasma, LCD and CRT displays
- Supports color key overlay
- Packed pixel memory organization, 8-bpp or 16bpp (1byte/pixel, 2byte per pixel available for TFT displays)
- Simple software interface, few control registers
- Versatile and programmable sync signals timing
- Single clock input for many displays
- Tested with more than 50 popular displays
- Display power-on sequencing control signals

Table 1: Example Implementation Statistics

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT/DSP48	DCM	MGT	PPC	Design Tools
Spartan-3™	XC3S1000-5	74	766	299	3	1	0	0	N/A	N/A	ISE 8.1.03i
Spartan-3E™	XC3S1600E-5	79	766	299	3	1	0	0	N/A	N/A	ISE 8.1.03i
Virtex-II Pro™	XC2VP4-5	94	761	299	3	1	0	0	0	0	ISE 8.1.03i
Virtex-4™	XC4VLX15-12	152	765	299	3	1	0	0	N/A	N/A	ISE 8.1.03i
Spartan-II E™	XC2S400E-7	57	762	299	3	1	0	N/A	N/A	N/A	ISE 8.1.03i

Notes:

- 1) Assuming 16-bit memory interface, 8-bit TFT LCD interface
- 2) Assuming all core I/Os and clocks are routed off-chip

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AllianceCORE™ Facts	
Provided with Core	
Documentation	User Guide
Design File Formats	NGC netlist, VHDL sources available at extra cost
Constraints Files	logiCVC.ucf
Verification	VHDL test bench
Instantiation templates	VHDL
Reference designs & application notes	Reference VHDL design, Application Notes
Additional Items	logiCRAFT2 Demo Board
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon d.o.o.	

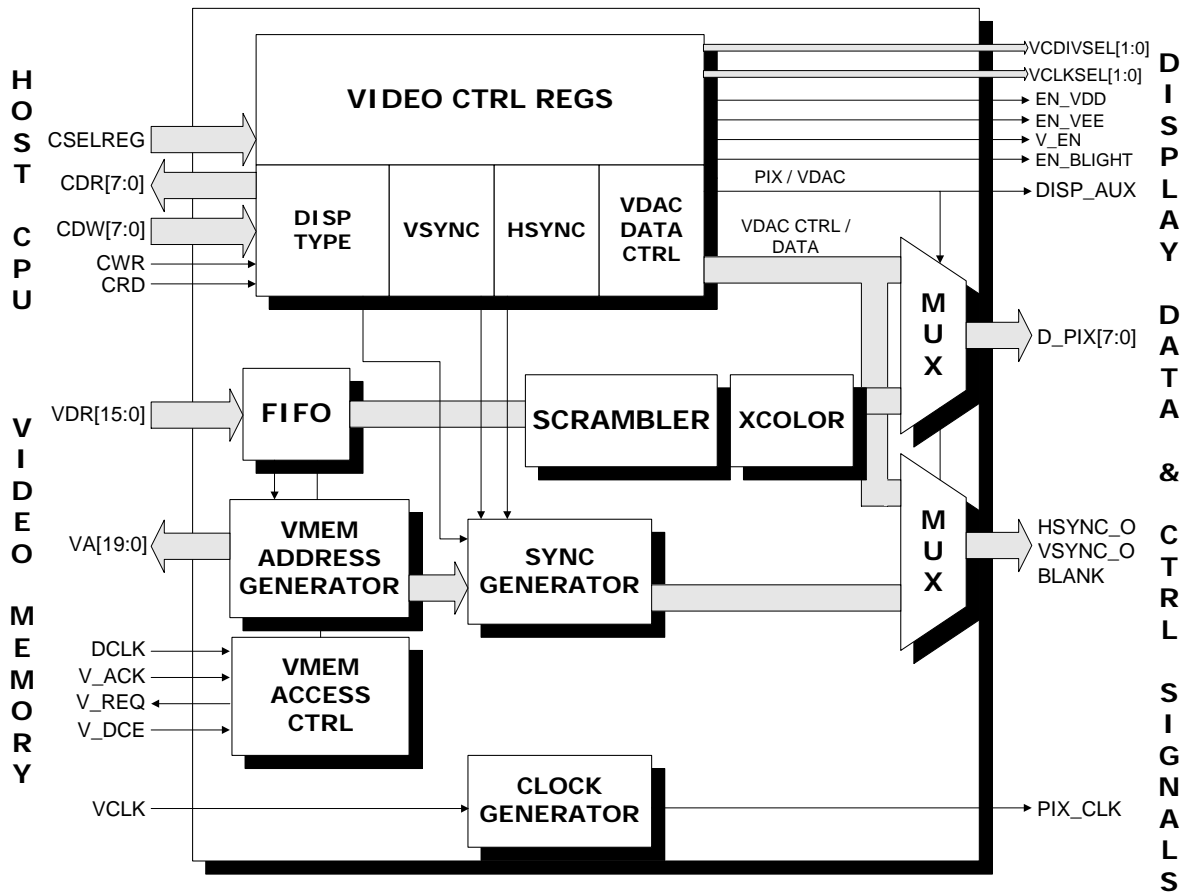


Figure 1: logiCVC Block Diagram

Features (continued)

- Optimized for SDRAM/DDRAM Video memory
- Synchronization on external video syncs
- Additional options :
 - SDRAM, DDRAM, SRAM video memory controller
 - Cost sensitive applications: UMA (unified memory architecture), programmable pixel row stripe, programmable pixel width
 - BitBlt graphic accelerator
 - logiWIN Versatile Video Input IP

Applications

- AutoPC, Personal Digital Assistants, Hand-Held PC, SetTop Boxes
- Human Machine Interfaces, Video Phones, Electronic Gadgets

General Description

The logiCVC – Compact Video Controller is a graphic video controller. Its functions include refreshing the display image by reading the video memory, converting the read data into a data stream acceptable for display interface, generating the control signals for display and providing the host (CPU) access to video memory. Optional processing functions, like bit-blit unit and character generator, can be easily supplemented.

The logiCVC controls flat panel displays, e.g., various LCD technologies (TNM, STNM, TFT, analogous RGB TFT), electroluminescent displays and plasma displays. By means of external video DAC or DVI drivers, it can also control CRT displays (i.e. VGA monitors) and DVI compliant monitors.

Both black-and-white and color displays up to 256 colors can be controlled by the logiCVC, while the XCOLOR™ technique provides up to 8 levels of gray for B/W and 256 color levels for color displays with 1 bit per color respectively. The XCOLOR™ technique generates color shades by switching on and off the adjoining pixels in different time slices.

The fact that only 23 eight-bit registers are required to control the video display simplifies the programming immensely. The frame buffer, or the video memory, is implemented in SDRAM. Due to SDRAM's high memory bandwidth, the video memory can also be used as a CPU working memory.

This type of hardware architecture is known as UMA (Unified Memory Architecture) and is extremely efficient in the implementation of low cost systems.

Functional Description

The logiCVC core contains several functional blocks: video memory access block, video control register block, clock generator unit, video data scrambler and video display synchronization signals generator.

Video Memory Access Block

The Video memory access block is comprised of three sub-blocks: video memory address generator, video memory handshake logic, and data FIFO. The video memory handshake logic issues a request to the SDRAM controller for memory access, while the address generator provides the memory address from which video data contents will be read into the video data FIFO. The function of data FIFO is to enable the optimal use of memory (SDRAM) bandwidth. Another function of the video memory handshake logic is to control the FIFO write and video memory address increment.

Video Control Register Block

The control registers contained in the video control register block form three groups: horizontal sync registers, vertical sync registers, and display type control registers.

Horizontal Sync Registers

These are horizontal front porch, back porch, resolution and sync registers. These registers control horizontal synchronization timing in pixel clock increments, such as HSYNC active state, delay from HSYNC inactive to data start, data length and delay from end of data up to HSYNC active.

Vertical Sync Registers

These are vertical front porch, back porch, resolution, and sync registers. These registers control vertical synchronization timing in pixel row increments, such as VSYNC active state, delay from VSYNC inactive to first visible pixel row start, number of visible rows and delay from last pixel row up to HSYNC active.

Display Type Control Registers

There are five registers used for programming different display types. They are Display Type1, Display Type2, Display Control, Second Panel Start, Video DAC Control/Data. Furthermore, single and double panel display types are also supported. The start address of the second panel image in video memory is specified in the second panel register for double panels.

The basic display clock frequency is determined by writing in Display Type1 register. The register Display Type2 is used to determine the polarity of display control signals, as well as to set them into a fixed logical state. Another function of this register is to control the generation of display control signals for special display types.

All display signals can be set into a tree-state, and additional control bits can be used to control the turning on and off of the individual display power supply. Video DAC register is used to control the VDAC for CRT displays. The same data and control display signals are used for VDAC programming and control. As a consequence, the number of control signals for all display types is reduced and unified.

Core Modifications

The core is supplied in a netlist format, with simulation vectors. The logiCVC source code (VHDL sources) is available at additional cost from Xylon.

Although the logiCVC has been constructed with regard to adaptability to various display types, and has been tested on a several popular displays (see Table 2), there may be instances where the source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiCVC core or to supplement some of your specific functions, order the source code or allow us to tailor the logiCVC to your requirements.

Table 2: Partial list of displays tested with the logiCVC

Display	Producer	Resolution
LM57QB1T04	Sharp	320x240 B/W
CLM480320A	Densitron	480x320 B/W
LMG9520	Sharp	320x240 ColSTN
LM057QC1T01	Sharp	320x240 ColSTN
LQ057Q3DC02	Sharp	320x240 Col TFT
LM7M632	Sharp	640x240 ColSTN
LJ64H034	Sharp	640x400 Elumin.
LM64P831	Sharp	640x480 B/W
LM64C350	Sharp	640x480 Col STN
NL6448AC33	NEC	640x480 Col TFT
LQ10D36	Sharp	640x480 Col TFT
LQ121S1DG11	Sharp	800x600 Col TFT
LQ150X1DG11	Sharp	1024x768 Col TFT
Various proprietary automotive displays		800x480 TFT 400x234 TFT
CRT		640x480 / 800x600 VGA

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Memory Interface		
VDR[MEM_DATA_WIDTH-1:0]	input	Video memory data
VA[ADDRSIZE-1:0]	output	Video memory addresses
V_REQ	output	Video request data
V_ACK	input	Reset video request
V_DCE	input	Video data available
V_BURST[MEM_BURST_WIDTH-	output	Video memory access burst length

1:0]		
DCLK	input	Memory interface clock
Display Control Signals		
HSYNC_O	output	Horizontal sync
VSYNC_O	output	Vertical sync
PIX_CLK	output	Pixel clock
BLANK	output	Blank/display enable at TFT
DISP_AUX	output	Auxiliary flag for CRT VDAC
D_PIX[VIDEO_DATA_WIDTH-1:0]	output	Video pixel data bus
Auxiliary Signals		
GSR	input	Global set/reset
VCLK	input	Video clock input
ENABLE_M	output	BLANK/DISP_AUX mux select
LINE_2K	output	1k or 2k pixel row length
BPP16_8	output	(BPP16_8 = 1) 16 bpp (BPP16_8 = 0) 8 bpp
FRAME_SYNC	output	Video page switching synchronization
OVERLAY_EN	input	Enable overlay function
OVERLAY_MUX	output	External analog mux control (used for overlay)
E_VSYNC	input	External VSYNC (used for resynchronization)
E_HSYNC_FALL	input	Falling edge of external HSYNC (used for resynchronization)
E_VIDEO_NOT_PRESENT	input	External video not present flag
E_VIDEO_SYNCHRONIZED	output	CVC synchronized on external video signal
ERR_FIFO_EMPTY	output	Video FIFO empty error flag
ERR_FIFO_CRITICAL	output	Video FIFO critical error flag (err_critical mark)
VCDIVSEL[1:0]	output	Video clock divider select
VCLKSEL[1:0]	output	Video clock select
EN_VDD	output	Enable Vdd power supply
EN_VEE	output	Enable Vee power supply
EN_BLIGHT	output	Enable backlight power supply
V_EN	output	Enable display control/data signals
CPU Control Signals		
CWR	input	CPU write
CRD	input	CPU read
REG_CLK	input	register clock
CDR[7:0]	output	CPU read data bus
CDW[7:0]	input	CPU write data bus
SHSY_FP	input	Hsync front porch register select
SHSY	input	Hsync active register select
SHSY_BP	input	Hsync back porch register select
SHSY_RESL	input	Hsync resolution low register select
SHSY_RESH	input	Hsync resolution high register select
SVSY_FP	input	Vsync front porch register select
SVSY	input	Vsync active register select
SVSY_BP	input	Vsync back porch register select
SVSY_RESL	input	Vsync low resolution register select
SVSY_RESH	input	Vsync high resolution register select
SCTRL1	input	Video control1 register select

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SCTRL2	input	Video control2 register select
SL_SCREENL	input	Lower screen (overlay image) start address low register select
SL_SCREENM	input	Lower screen (overlay image) start address middle register select
SL_SCREENH	input	Lower screen (overlay image) start address high register select
SDTYPE1	input	Display type1 register select
SDTYPE2	input	Display type2 register select
SVDAC	input	Video DAC data register select
SM	input	Alternate clock register select
SPWRCTRL	input	Power control register select
SOVERLAYL	input	Overlay color key register (lower) select
SOVERLAYH	input	Overlay color key register (higher) select
SXCOLOR	input	XCOLOR register select
HSY_FP[7:0]	output	Hsync front porch register read bus
HSY[7:0]	output	Hsync active register read bus
HSY_BP[7:0]	output	Hsync back porch register read bus
HSY_RESL[7:0]	output	Hsync resolution low register read bus
HSY_RESH[7:0]	output	Hsync resolution high register read bus
VSY_FP[7:0]	output	Vsync front porch register read bus
VSY[7:0]	output	Vsync active register read bus
VSY_BP[7:0]	output	Vsync back porch register read bus
VSY_RESL[7:0]	output	Vsync low resolution register read bus
VSY_RESH[7:0]	output	Vsync high resolution register read bus
CTRL1[7:0]	output	Video control1 register read bus
CTRL2[7:0]	output	Video control2 register read bus
L_SCREENL[7:0]	output	Lower screen (overlay image) start address low register read bus
L_SCREENM[7:0]	output	Lower screen (overlay image) start address middle register read bus
L_SCREENH[7:0]	output	Lower screen (overlay image) start address high register read bus
DTYPE1[7:0]	output	Display type1 register read bus
DTYPE2[7:0]	output	Display type2 register read bus
VDAC[7:0]	output	Video DAC data register read bus
M[7:0]	output	Alternate clock register read bus
PWRCTRL[7:0]	output	Power control register read bus
OVERLAYL[7:0]	output	Overlay color key register (lower) read bus
OVERLAYH[7:0]	output	Overlay color key register (higher) read bus

Available Support Products

All logicBRICKS™ IP cores can be evaluated, tested and used on Xylon's logiCRAFT2 Multimedia and Infotainment Evaluation/Development platform.

The logiCRAFT2 is Spartan-3™ centric platform capable of driving up to three displays. The platform can simultaneously display different video streams on each screen.

Besides unique display driving capabilities, the logiCRAFT2 supports many networking types. The logiCRAFT2 is expandable and enables rapid hardware prototyping.

Detailed logiCRAFT2 info can be found at www.logicbricks.com.

Verification Methods

The logiCVC IP core is instantiated into the VHDL test-bench as an UUT (Unit Under Test). The test-bench simulates all required hardware modules and processes: clock generation, whole memory subsystem and the register interface. The logiCVC can be easily re-initialized for different video displays

and its response can be simply checked against the video display's specifications. Initialization parameters and the image patterns for several popular displays are supplied.

Along with the logiCVC core, user instructions are provided for a step-by-step core simulation, as well as for the core integration. The instructions are particularly relevant for new IP cores and Xilinx tools users.

The logiCVC has been developed as the part of a larger design. It has been tested in several designs, and proved in large-scale production.

Recommended Design Experience

The users should have experience in the following areas:

- Synchronous digital circuit design
- Xilinx ISE tools
- ModelSim

Ordering Information

This product is available directly from Xilinx Alliance Program member Xylon under the terms of the SignOnce IP License. Please contact Xylon for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Xylon or visit the web:

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Related Information

Xilinx Programmable Logic

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