Summary

This white paper presents details of the new Xylon licensing model that applies to Xylon's logicBRICKS™ IP cores for Xilinx® FPGAs. This new IP licensing model has been developed for IP users designing Xilinx FPGA based products for production volumes in the range of 1 - 5,000 units or similar. IP cores' costs per product unit (IP cost/unit) in such low production volumes are usually too high to justify investments into third-party IP cores, or even to the FPGA silicon and associated NRE costs. Xylon's Low-Volume IP Program uses licensing model that changes the existing market paradigm. This program typically lowers the IP cost/unit ratio up to ten times. The model maximally simplifies the licensing procedure and enables IP users to purchase the logicBRICKS IP cores at a price equivalent to or less than the cost of one engineer per week. Low-cost Xylon IP products virtually eliminate a need for an in-house IP development. Included technical support additionally speeds up developments of Xilinx FPGA designs featuring logicBRICKS IP cores. This new Low-Volume IP program shortens the time required for the development of FPGA and the time-to-market window, while at the same time significantly reduces development costs. All logicBRICKS IP cores are fully integrated into Xilinx Platform Studio and the EDK toolkit, and designers that are familiar with these tools can immediately start designing with the logicBRICKS.

IP Cores in Xilinx FPGA Design

Today's FPGA technology provides more features and more design possibilities to FPGA designers and system integrators than ever before. Utilized FPGA designs have rapidly changed from simple glue logic implementations into full Systems-On-a-Chip (SOC). This substantial change has created an old designers' problem well known in the ASIC industry – the design productivity gap. New development tools can speed up modern FPGA developments. Automatic code generators that reduce the required amount of hand-coding, newer and faster digital and analog simulators, synthesis and implementation tools, etc., certainly enable designers to do more in less time.

However, designing from a scratch has not been a viable approach in designing advanced FPGA systems for a while. A quality step that fills the FPGA design productivity gap is adoption of predefined and reusable function blocks into the design flow. The blocks, called IP cores, enable designers to concentrate on missing SoC system parts, shorten development times, design risks and costs. Although benefits of using IP cores in FPGA chip developments have been known for many years, the FPGA IP cores' market has not followed the ASIC IP core market's development paradigm. There are several reasons that slowed down expansion of the FPGA IP market.

IP core providers must put an extensive amount of efforts in development of a reusable IP core. The core must be highly configurable, in-depth tested and verified, and provided with rich and various deliverables to enable end-users to easily customize it and implement in FPGAs.

The IP production is demanding and costly. Providers must make revenues from IP core products, which is quite demanding due to a relatively small user base. High IP cores' prices forestall significant user base expansion and the growth of the overall FPGA IP core market.

At the same time IP core users look for IP cores with appropriate feature sets that can be seamlessly integrated into targeted designs. IP prices must favor third-party IP cores against in-house developments. Considering that a typical FPGA design usually requires more IP cores, it is understandable that purchasing of third-party IP cores can be challenging even for a very well funded companies. The bare price of the IP core is just a part of overall costs, since users must invest time, technical skills and accept design risks. Due to these reasons, an easy use and short learning time are of the highest importance.

Xilinx, Inc., the global leader in programmable logic solutions, have changed the described trend by introducing advanced Xilinx Platform Studio and the Embedded Development Kit (EDK) development tools and related silicon and software products. The EDK is an integrated development environment for designing embedded processing systems. It includes Xilinx Platform Studio and the Software Development kit, as well as a rich library of IP cores. These technologies have helped Xilinx users to take on IP cores reuse, and have setup new standards to independent third-party IP providers. New Xilinx tools and a new approach to embedded systems design have solved an old IP reuse problem of non-standardized SoC bussing structures. Xilinx has adopted IBM CoreConnect architecture that sets up a standard to third-party IP providers. Accordingly to the announcement from the December 2009, the company plan to adopt a well known ARM AMBA bus architecture as well.

Sophisticated EDK GUI interface, allowing for an easy system design and IP configuration, has made the FPGA design easier even to FPGA users with a small or nonexistent FPGA experience.

Xylon's logicBRICKS IP Cores

Since the establishment in 1995, Xylon is being focused on developments of embedded systems based on Xilinx technologies and development of IP cores for Xilinx FPGAs. Company's special fields of interest are embedded graphics, video and networking.

Extensive experience in FPGA design has initiated production of Xylon IP cores for the open market. Xylon established the library of IP cores named logicBRICKS in the year 2000. A year later, the company joined the Xilinx Alliance Program.

Before the emergence of Xilinx Platform Studio and the Embedded Development Kit (EDK) development tools, the IP cores trading was quite clumsy and impractical for both parties, third-party providers and IP users. Non standardized on-chip bus structures have created a lot of problems in the market of IP cores for the Xilinx FPGA, as well as in other FPGA markets. Ready-to-Use IP products have often had bus interfaces incompatible to a rest of potential user's design. This fact, although technically solvable, often created a barrier between IP providers and end users. A significant design time had to be spent on third-party IP cores adoption to the targeted design.

At that time Xylon's logicBRICKS and other third-party providers' IP cores have been productized in the "black-box" form and traded as industry standard EDIF or Xilinx NGC formatted netlist files. This IP core format is not very flexible and does not allow for easy IP changes. Third-party IP providers working with the "black-box" IP cores have problems in managing design and sales, spending additional designers hours on IP customizations, etc. End IP users of "black–box" IP cores have difficulties in adopting technology, spending designers' hours on learning about other companies' products, have issues regarding a large dependence on the IP provider, etc. The "black-box" IP form does not provide enough intellectual property's security to IP providers and IP users. The providers' problem is prevention of netlists' backannotation and reverse engineering. The end users usually have problems of giving third-party providers insights into their own designs during the IP customization phase.

Xilinx Platform Studio and the Embedded Development Kit (EDK) development tools have tremendously changed the described situation. Xilinx has introduced new device families with integrated hard-core PowerPC microprocessors supporting the IBM CoreConnectTM PLB and OPB bus architecture. Xilinx soft-CPU MicroBlazeTM RISC microprocessor has enabled an embedded computing even in the low-cost Xilinx FPGA families integratint the CoreConnect bus.

Xylon has immediately adopted logicBRICKS IP cores to the described Xilinx technologies, and created IP cores that enable users to stay a step ahead of competitors. The logicBRICKS IP cores are fully supported by the Xilinx Platform Studio and the EDK integrated software solution, which enables an immediate start to FPGA designers familiar with Xilinx tools. The logicBRICKS allow for configuration through graphical user interface and implementation of targeted SoCs without hand coding. All logicBRICKS IP cores come with a detailed documentation, software support and reference designs. The cores are provided in an encrypted VHDL format that protects Xylon's intellectual property and allows a great designing freedom to logicBRICKS users.

The following table summarizes main IP users' requirements and Xylon's answers to the requirements. It should be noted that some licensing rights granted by the Low-Volume IP program differ from rights and conditions granted by other Xylon licensing models. Table 2 describes differences between Xylon's licensing models.

IP Users' requirements	Xylon's Answer
Excellent IP performances	logicBRICKS IP cores are exclusively optimized for Xilinx FPGA architectures and fully exploit available silicon resources. As a dedicated provider of IP cores for Xilinx FPGAs, Xylon is investing great efforts to stay aligned with the latest technology developments and to provide the best IP solutions that rationally consume targeted chips' resources. Xylon does not produce generic HDL IP cores, which do not utilize special Xilinx chips' features.
Easy of Use	logicBRICKS IP cores are fully compatible to the Xilinx Platform Studio and the EDK. Users can use the logicBRICKS in the exactly same ways as Xilinx IP cores. It means that there is no additional learning time and that FPGA designers can immediately start designing with the logicBRICKS.
Simple parameterization with no assistance from the IP provider	The EDK GUI interface enables an easy parameterization (customization) of the logicBRICKS IP cores, and exact setup of requested IP cores' features. Hand-coding is not required.
First-class Technical Support	logicBRICKS IP users get an access to a strong technical support assured by Xylon. The technical support is provided during a period defined with particular license agreement, and can be prolonged on demand. Xylon technical support provides a direct link to skilled engineers who can assist in a timely and satisfying way.
IP customization on request	Standard logicBRICKS IP products are prepared for Xilinx EDK tools, but customers may want to have Xilinx ISE compliant versions optimized for the smallest possible FPGA silicon utilization. Xylon customers can engage Xyon's design services for logicBRICKS customizations.
Try-before-Buy possibility and product evaluation through all implementation phases	Xylon provides evaluation logicBRICKS IP cores. The evaluation versions are run-time limited and functionally equal to fully licensed products. Interested buyers can try the logicBRICKS through all stages of the FPGA implementation flow.
Simple and flexible license model	Xylon endorses Xilinx's SignOnce licensing and offers Site or Project license types. These licensing types are available to customers that plan logicBRICKS use in mid and high FPGA product volumes. The Low-Volume IP program offers a new licensing mechanism that enable users to purchase and license the logicBRICKS IP cores within minutes. Other licensing types are optional.
Referent hardware platforms	Xylon offers several logiCRAFT HW evaluation platforms, which can be used for evaluation of the logicBRICKS IP cores, as well as for the product development and prototyping purposes. Xylon logicBRICKS evaluation IP cores can be used on other HW platforms, i.e. Xilinx evaluation boards, with no limitations except those described in the licensing agreement.
Reliable supplier with Industrial references	Xylon has being operating since 1995 and has good industry references. Xylon products are built into electronic devices which have been in worldwide use for years, and have gone through rigorous tests in the industrial production of electronic equipment besides usual IP verification methods.
Acceptable price	Xylon logicBRICKS IP cores provides all the benefits of third-party IP cores that users are asking for. This document describes the new Xylon's Low-Volume IP program that allows users to buy full IP licenses at the price lower than a week of engineering time.

Table 1: The Most Important Third-Party IP Features

logicBRICKS Design Flow

Xylon's customers can purchase logicBRICKS IP cores in different ways: by contacting Xylon sales at sales@logicbricks.com, through a network of distributers, or online (Xylon's web shop). The logicBRICKS users get the logicBRICKS IP cores in a format compliant to the Xilinx Platform Studio and the EDK.

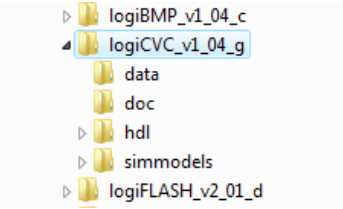


Figure 1: The IP folder structure

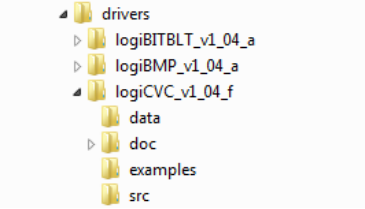


Figure 2: The IP driver folder structure

Figure 1 presents the folder structure of a typical logicBRICKS IP core. Figure 2 presents the folder structure of associated IP software driver. Xilinx EDK users are familiar with this IP structure.

logicBRICKS in the EDK IP Catalogue

The logicBRICKS IP cores must be stored into default, or user setup Xilinx EDK project's Project Peripheral Repository. It enables the EDK to find the Xylon logicBRICKS IP cores and display them in the IP catalog. The following figure displays a number of the logicBRICKS IP cores imported in the IP catalogue and ready for implementation.

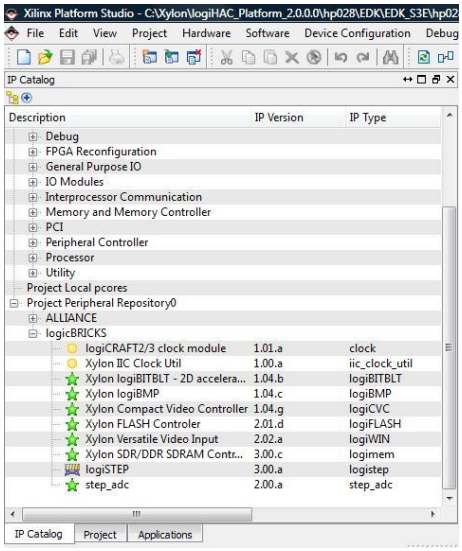


Figure 3: The logicBRICKS in the EDK IP Catalogue

Connecting logicBRICKS to the Xilinx SoC Design

EDK users can simply drag and drop the logicBRICKS IP cores from the EDK IP catalogue into the System Assembly View area. Figure 4 shows an example Xilinx FPGA design utilizing several Xylon's IP cores. Users can connect the logicBRICKS IP core to the rest of the System-On-a-Chip design by just several mouse clicks. The figure shows the logicBRICKS IP cores connected to the on-chip CoreConnect PLB bus.

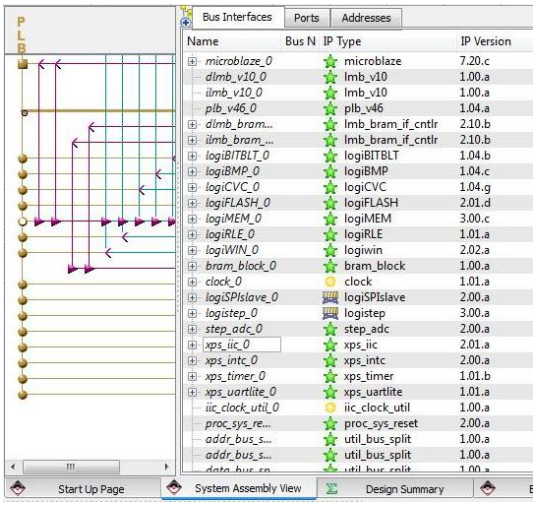


Figure 4: The logicBRICKS IPs Integrated in the EDK FPGA Design

Setting up the logicBRICKS IP Parameters

logicBRICKS IP cores can be simply configured through the EDK GUI. A mouse double click on the logicBRICKS IP icon within the EDK System Assembly View opens the IP's GUI. The GUI allows for changes of provided user-changeable IP parameters. Figure 5 provides a detail of the scrollable GUI parameters list for the logicBRICKS logiCVC-ML Compact Multilayer Video Controller IP core. The provided detail illustrates how users can easily change i.e. the number of graphics layers supported by the logiCVC-ML, or the pixel color depth that can be independently setup for each graphics layer, etc.

All logicBRICKS IP cores can be parameterized (configured) in the same way. It allows users to setup an exact IP features set prior to a design's synthesis. The selected features setup directly affects the consumption of available Xilinx FPGA silicon resources. Removal of unwanted IP's features assures smaller IP implementation and silicon resources savings.

Upon the definition of internal FPGA architecture and interfaces, the FPGA should be implemented as it is being described by related Xilinx documentation.

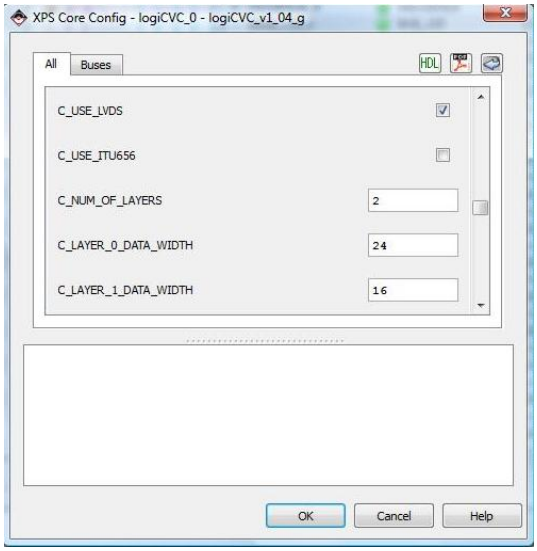


Figure 5: The logicBRICKS logiCVC-ML IP core GUI (a detail)

The described GUI enables an easy access to logicBRICKS IP cores' documentation provided in the portable PDF format.

Xylon's Low-Volume IP Program

Ten years of operation in a role of third-party IP provider for the open market has allowed Xylon to get an insight into needs of typical FPGA users and their IP requirements. We have carefully analyzed inputs from potential customers to accurately detect what elements of our products and business models must change to make logicBRICKS IP cores more acceptable and affordable.

This analysis has helped us to create the new logicBRICKS IP licensing model, which presents the news on the market of third-party IP cores for the Xilinx FPGAs.

This new logicBRICKS IP licensing model has been created for IP users designing Xilinx FPGA based products for production volumes in a range 1 - 10,000 units. A typical market IP core's price of €10,000 (price example for illustration purposes) presents a significant cost per product unit (IP cost/unit), if the total number of manufactured product units lies in the specified production volume range.

New Xylon licensing model significantly decreases IP license fees for the logicBRICKS IP cores, and consequently lower the IP cost/unit.

Actually, the license fees in this licensing program can cost as low as a single engineer per week!

Such a radical change of costs associated with Xylon logicBRICKS IP cores makes in-house developments of FPGA functions supported by the logicBRICKS hardly justified.

The following table provides a quick overview of differences between logicBRICKS licensing models for high-volume and the low-volume FPGA products.

	Xylon Standard Licensing Model	Xylon Low-Volume Licensing Model
Number of manufactured units	No limit	5,000 units (basic license) Expandable: 10K, 20K, 50K, 100K, or no limit
License Type	Perpetual	Time-Based
License Contract	Paper form (SignOnce or similar)	Online (Click Form) Offline (Part of IP deliverables)
License Fee	Contact sales@logicbricks.com	Up to 10 times lower (prices start at €500)*1
License Duration	No limit	Defined by a license: 1, 2, or 3 years*2*3
Developer seats limitation	No limit at the specified geographic location	1 seat
Included Tech Support	Defined by contract	A number of e-mail hours support*4 included with every logicBRICKS IP core
Additional Tech Support	Extendable for a number of years	Additional 10 hours support packages
Customer's report	Not required	Production Volume Report filled annually
Sales Channel	Xylon and Representatives, Distributors	Online 24 hours/day, 7 days/week Offline: Xylon and distributors
Lead Time	days	minutes
Payment	As agreed	Credit Cards, wire transfer, PayPal, etc. Other payment types can be arranged

**1 – Xylon offers some IP cores at specially discounted prices that may be lower that the indicated one. Please visit www.logicbricks.com to learn more.*

**2 – Due to some technical limitations actual licenses' duration is 360, 720 and 1080 days, respectively.*

**3 – The Low-Volume license does not constrain system's production to a time defined by the license agreement i.e., 1 year. Developed products can be manufactured after license's expiration.*

**4 – Check http://www.logicbricks.com/logicBRICKS_IP_Library/Included_LVIP_Tech_Support.aspx for an exact number of included technical support hours for particular IP core*

Table 2: Xylon Licensing Models Comparison

Cost Benefits

A simple cost per unit analysis, provided by the following table, clearly shows how the logicBRICKS IP users benefit from the new Low-Volume IP Program.

	Xylon Standard Licensing Model	Xylon Low-Volume Licensing Model
License Fee[*1]	€10,000	€1,000
No of Units	2,000	2,000
IP Cost/Unit	€5/unit	€0.5/unit

**1 – IP pricing used for illustration purposes only. Please contact sales@logicbricks.com for exact to learn more about the logicBRICKS pricing, or visit www.logicbricks.com.*

Table 3: IP Cost per System Unit

Depending on the IP type and the desired functionality, the €5/unit cost bundled to the IP core, can be noncompetitive to ASSP solutions or in-house developments. The last column in the table shows that the logicBRICKS IP core can be purchased for an amount smaller than a typical engineer/week cost. The IP cost/units can be decreased up to ten times.

Product

The logicBRICKS IP cores, supplied with the new license, are identical to the logicBRICKS IP cores licensed by other Xylon licensing types. All differences relate to the licensing model itself and there are no functional differences.

For a price of an engineer/week, the logicBRICKS buyers can get sophisticated IP core products integrating many engineer/years of development.

At the moment, Xylon does not provide the full logicBRICKS IP library with the new licensing model. The model shall apply to all logicBRICKS IP cores in a near future.

Purchasing and Licensing Procedure

This paragraph provides a general overview of purchasing and licensing, which can be accomplished online and in just a few minutes.

Step No.	Purchasing and Licensing
1	Customers can visit Xylon web shop at www.logicbricks.com, and add the desired logicBRICKS IP core into the Shopping Cart. Click on the BUY icon activates a link towards the Share It! online sell web page. Xylon partners with the share It! (www.shareit.com), global E-commerce company, in order to assure the highest shopping convenience and security to the customers. The logicBRICKS IP cores can be paid by all types of money transfer supported by Share It!, such as Credit card, wire transfer, PayPal, etc.
2	Upon the payment, Xylon sends confirmation e-mail with licensing and downloading instructions. The IP deliverables can be downloaded from the Xylon's web.
3	Within the Xylon registration area, the user must provide the PC MAC (Media Access Control address) or SUN Host ID, which uniquely identifies the user's workstation. The logicBRICKS IP license is bonded to a single workstation.
4	Xylon sends e-mail with the IP license and license installation instructions.
5	The user installs the license on the workstation (PC or SUN). The logicBRICKS IP core is successfully installed and ready for use as described in the paragraph: *logicBRICKS Design Flow*.

Table 4: Purchasing and Licensing Overview

The logicBRICKS IP cores are available for purchase seven days a week and 24 hours a day!

Technical Support

Every Low-Volume IP license includes a number of technical support hours. The technical support is provided by an e-mail. Exact number of provided tech support hours for every logicBRICKS IP core can be checked at http://www.logicbricks.com/logicBRICKS_IP_Library/Included_LVIP_Tech_Support.aspx.

Multiple logicBRICKS IP licenses (different IP cores) allow customers to use all included technical support hours for any IP core at their preferences. It means that i.e., valid licenses for the logiCVC-ML Compact Multilayered Video Controller and the logiWIN Versatile Video Input IP cores, allow the customer to spend i.e 20 hours of support on a single core, or to split the available technical support hours on both cores at any proportion.

Customers who need more technical support can purchase additional technical support hours.

Additional Bitstreams

Standard Low-Volume IP Program license grants buyer rights to produce 5,000 system units with the Xilinx FPGA integrating logicBRICKS IP cores.

Buyers who need higher production volumes can purchase additional production rights, or additional bitstream usage rights, in the following steps:

- 10,000 system units
- 20,000 system units
- 50,000 system units
- 100,000 system units
- Unlimited production

Xylon Development and Evaluation HW Platforms

The logicBRICKS IP cores can be evaluated on several evaluation and development platforms designed and manufactured by Xylon. These platforms are designed especially for developers working in the fields of multimedia and infotainment. All Xylon platforms demonstrate modularity at all levels: software, PCB board, FPGA, and IP cores.

The platforms make excellent development tools appropriate for development of embedded systems with strong graphics capabilities. Xylon platforms support a variety of audio and video sources, and handle a variety of LCD display types.

Platform	Description
	**logiCRAFT6 Multimedia Evaluation/Development Platform** The logiCRAFT6 Multimedia Evaluation and Development Platform based on the Xilinx® Spartan®-6 is a replacement for the older Xylon's logiCRAFT3 hardware platform. http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2562&sifraCvor=415
	**logiCRAFT-CC Companion Chip Platform** This Xilinx Spartan®-6 based development platform highlights the flexibility of FPGA based companion chips for popular embedded host processors. Embedded designers can expand, upgrade and differentiate systems by adding the FPGA to the host processor. The FPGA can support missing processor features and specialized interfacing. Additionally, high-speed processing can be offloaded from the processor. The logiCRAFT-CC has a rich software support to enable interfacing with the most complex embedded processors running different OSes. *http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2554&sifraCvor=415*

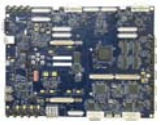
	**logiTAP Platform for Embedded GUI Developments:** This platform based on the Xilinx Spartan-3E offers a complete design framework for embedded designers developing GUI applications. The platform comes packed into a single Plexiglas casing and uses a high resolution color LCD touch display as the user interface. The logiTAP works with several third-party GUI builder tools allowing for a full set of graphics rendering features. *http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2339&sifraCvor=415*
	**logiHAC Automotive Hybrid Cluster Development Platform:** This Xilinx Spartan-3E based platform enables developments of hybrid instrument clusters integrating analog-type gauges and a high resolution TFT LCD display. A low-cost Microchip PIC MCU controls FPGA graphics/steppers controller implemented by Xylon logicBRICKS and Xilinx IP cores. The presented Xylon FPGA controller can be connected to virtually any microcontroller. http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2340&sifraCvor=415
	**logiCRAFT3 Compact Multimedia Display Development Platform:** The logiCRAFT3 is Xylon small-factor configurable platform designed to support a wide variety of audio and video sources. The board can drive a variety of display types. The logiCRAFT3 integrates several standard communication interfaces enabling an easy programming and control, as well as a smooth integration into larger systems. http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2341&sifraCvor=415
	**logiCRAFT2 Multimedia Evaluation/Development Platform:** The logiCRAFT2 Xilinx Spartan-3 based demonstration and development platform is designed for developers working in a field of multimedia and infotainment. The platform demonstrates modularity on all levels and provides customers with flexibility, fast development cycles, and lower development and production costs. http://www.logicbricks.com/Product/Detail.aspx?sifraProizvod=2342&sifraCvor=415

Table 5: Xylon HW Platforms

Revision History

Version	Date	Note
1.00	14.01.2010.	Initial release with edited hyperlinks.

Xylon d.o.o.
Fallerovo setaliste 22,
10000 Zagreb, Croatia
www.logicbricks.com