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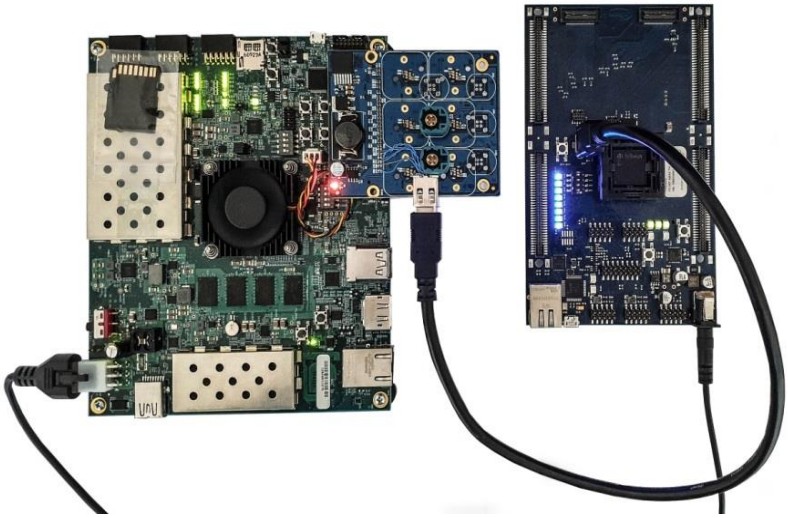

Figure 1: logiHSSL-ZU FPGA HSSL Starter Kit

Features

- Combines Infineon's AURIX™ microcontroller and Xilinx® Zynq® UltraScale+™ MPSoC programmable device
- Integrates Infineon High Sped Serial Link (HSSL) optimized for Xilinx FPGA implementations
- Includes the complete reference design with the evaluation logicBRICKS IP cores:
  - logiHSSL Slave HSSL Controller
- Linked devices can access and control each other's resources
- Complete hardware platform includes:
  - 1x Xilinx Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit
  - 1x Infineon Aurix Evaluation Board Kit KIT_A2G_TC397_S_TR
  - 1x Xylon FMC board for cable connection
  - 1x FireWire cable
- Design is prepared for Xilinx Vivado® Design Suite
- Documentation and tech support (e-mail)

Applications

Emerging automotive and industrial applications, such as the Advanced Driver Assistance (ADAS) and Automated Driving (AD), that are both performance-hungry and safety-critical.

General Description

The logiHSSL-ZU FPGA HSSL Starter Kit designs provides system designers with everything they need to quickly interconnect the Infineon's AURIX™ microcontrollers with the Xilinx All Programmable FPGA and SoC devices via the Infineon High Speed Serial Link (HSSL). Combinations of these devices solve the rising safety and performance requirements in emerging automotive and industrial designs.

Kit deliverables include the complete reference design built around the logiHSSL Slave HSSL Controller IP core, which enables the linked devices to access and control each other's internal and connected resources. Like other Xylon's logicBRICKS IP cores, the logiHSSL is prepared for the Xilinx Vivado Design Suite and come with 1-month evaluation IP license, documentation and support.

The logiHSSL IP core enables the high-speed HSSL communication between microcontrollers of Infineon's TC2xx and TC3xx AURIX microcontrollers family and Xilinx SoC (System-on-Chip), MPSoC (MultiProcessor SoC) and FPGA (Field Programmable Gate Arrays). This serial link supports baudrates of up to 320 Mbaud at a net payload data-rate of up to 84%.

To learn more about the logiHSSL IP core, please visit https://www.logicbricks.com/Products/logiHSSL.aspx.

Design Framework

Hardware Design Files

- Configuration bitstream file for the programmable logic and the SDK export of the reference design that allows immediate start and software changes
- ZC706, ZCU102 and ZCU104 development board reference designs prepared for the Vivado Design Suite 2019.1
- Xylon evaluation logicBRICKS IP cores:
  - logiHSSL Slave HSSL Controller

Software

- logiHSSL application for set up and initialization of the logiHSSL IP core.

Binaries

- Precompiled SD card image for the fastest demo start-up
- First Stage Bootloader (FSBL)
- Standalone logiHSSL application example

Hardware

The logiHSSL-ZU Starter kit includes the following hardware parts:

- Xilinx Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit: https://www.xilinx.com/products/boards-and-kits/zcu104.html
- Infineon Aurix Evaluation Board Kit KIT_A2G_TC397_S_TR: https://www.infineon.com/cms/en/product/evaluation-boards/kit_a2g_tc397_s_trb/
- Xylon FMC board adapted for the FireWire cable connection
- FireWire cable – used only as a physical medium

Reference Design

The pre-verified reference design provides system designers with everything they need to quickly interconnect the Infineon's AURIX microcontrollers with the Xilinx All Programmable MPSoC device. The design is created by the Xilinx Vivado Design Suite and the SDK 2019.1 toolsets. The reference designs demonstrates bi-directional accesses between the logiHSSL IP and the on-board system DDR memory.

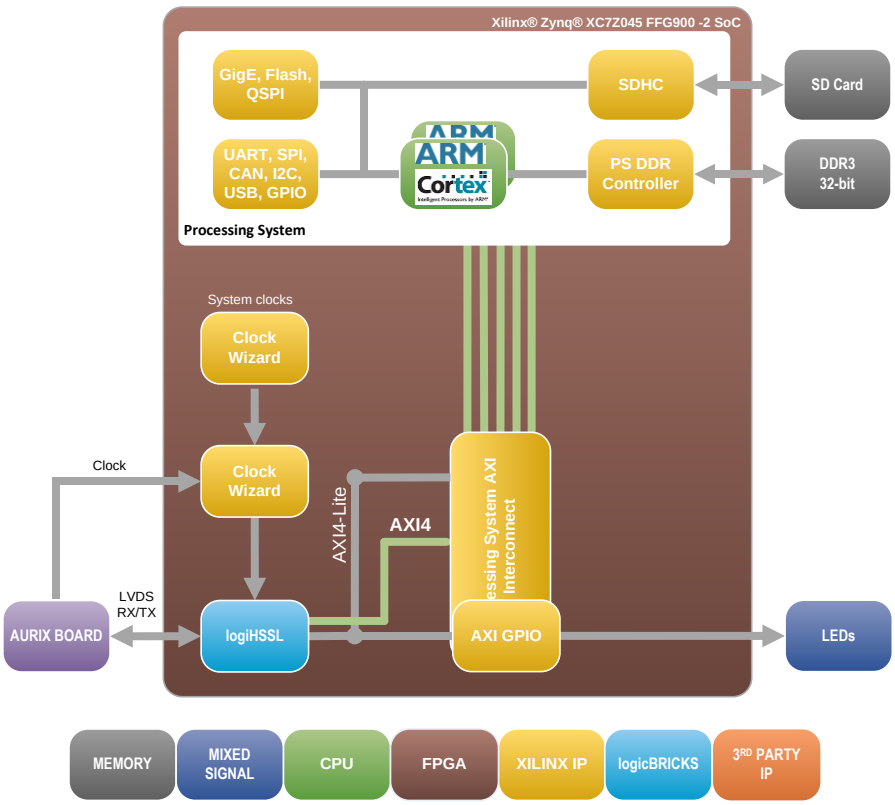

Figure 2: Reference Design Block Diagram

The logiHSSL IP core is connected to the AXI4 bus and users can modify design to enable the logiHSSL IP core accesses to other AXI4 addressable resources, such as other IP cores' register spaces, MIG controller, etc. All design clocks required for the logiHSSL IP core are generated by Xilinx Clock Wizard. The HSSL reference clock is selected between external and internal clock by the mux in the Clock Wizard. The below figure shows a detail from the reference design.

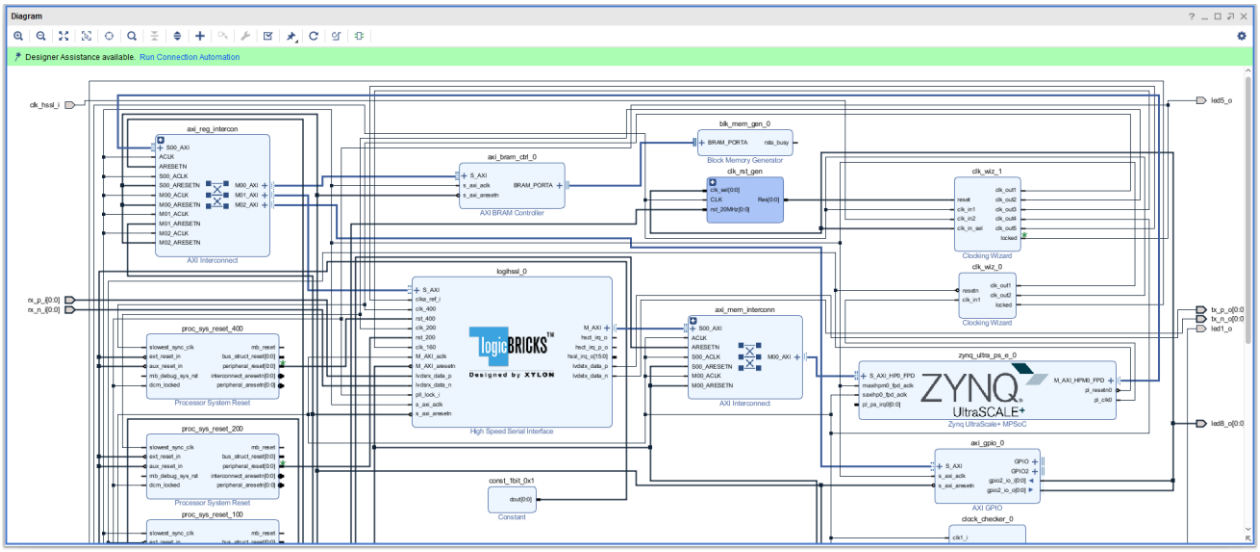

Figure 3: Implementing the logiHSSL in the Vivado Block Design

Available Support Products

Xylon logiHSSL IP core enables easy interfacing between Infineon's AURIX family (TC2xx and TC3xx) and Xilinx SoC (System-on-Chip), MPSoC (MultiProcessor SoC) and FPGA (Field Programmable Gate Arrays) devices via the Infineon High Speed Serial Link (HSSL). To learn more and get the IP core datasheet, please visit:

Email: sales@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHSSL.aspx

Ordering Information

This product is available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHSSL-ZU.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	02.12.2019.	Initial public release.
1.1	14.02.2020.	Update for release of HSSL IP v1.1.1