logicBRICKS
by Xylon

Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
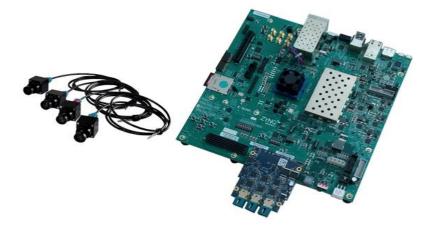URL: www.logicbricks.com

Figure 1: logiISP-ZU-GMSL2 HDR ISP Evaluation Kit

Features

- Complete and flexible HDR ISP Image Signal Processing design platform for embedded multi-camera vision and AI applications
- Based on Xilinx Zynq® UltraScale+™ MPSoC
- Includes licensed[1] logiREF-MULTICAM-ISP reference MPSoC designs with a complete logicBRICKS HDR ISP IP Suite
- Demonstrates a full HDR ISP pipeline for simultaneous processing of four automotive video cameras
- Resolutions: IN 1928x1208* and OUT 1920x1080
- The design is fully prepared for the Xilinx Vivado® Design Suite 2020.2
- The provided demo runs on Linux OS and includes logicBRICKS software drivers and applications prepared for the Xilinx Vitis™ Unified Software Platform 2020.2

- Compatible with Xilinx PetaLinux tools
- The kit supports the next generation GMSL2 high-speed serial interface from Maxim Integrated
- HDMI™ display output with the Xilinx HDMI 1.4/2.0 Transmitter Subsystem[2] controlled via Xylon's DRM kernel driver
- The complete hardware platform includes:

  - 1x Xilinx ZCU102 Evaluation Kit
  - 1x Xylon video input FMC board
  - 4x Xylon 2.3MP automotive video cameras
  - 4x Rosenberger® FAKRA cables (5 m)
  - 3x Rosenberger® HFM® to 4x FAKRA cable assembly
  - Power Supply

- Documentation and Tech support (e-mail)

1   Included 3-month Xylon seat evaluation licenses for used Xylon logicBRICKS IP cores.

2   Xilinx licensed IP. Digital code vouchers provided by Xylon to buyers of the logiISP-ZU-GMSL2 HDR ISP Evaluation Kit.

Applications

- AD/ADAS, AI, guided robotics, drones, machine vision, AR/VR and other vision applications

General Description

The logiISP-ZU-GMSL2 HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to efficiently develop multi-camera vision applications on Xilinx's Zynq UltraScale+ MPSoC devices. The complete hardware platform includes four of Xylon's 2.3MP automotive video cameras with the raw Bayer video output and supports the HDMI video output to control a monitor.

Kit deliverables include the complete and licensed logiREF-MULTICAM-ISP multi-camera HDR ISP pre-verified reference design implemented by Xylon's logicBRICKS IP cores. All IP cores are supplied with bare-metal and Linux software drivers. The video capture and display demo applications run in Linux OS.

Figure 2: Parallel HDR ISP Processing of 4x 2.3 MP Automotive Cameras by the logiREF-MULTICAM-ISP Reference Design

logiREF-MULTICAM-ISP Video Design Framework

The logiISP-ZU-GMSL2 reference design[1] includes Xylon's logicBRICKS IP cores and design files prepared for Xilinx's Vivado Design Suite. To get more information about the framework, please read the datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiREF-MULTICAM-ISP_hds.pdf.

This reference design demonstrates parallel video processing capabilities of Xylon's logicBRICKS HDR ISP pipeline and shows how, in comparison to simple instantiation of multiple ISP pipelines within a single programmable device, logicBRICKS IP cores allow for tremendous savings of up to 50 % of valuable programmable logic.

Key IP cores, the logiISP-UHD ISP pipeline and the logiHDR HDR pipeline, support parallel processing of multiple video inputs, resolutions up to 7680x7680 (including the popular 4K2Kp60 video resolution), merging of two or three exposures, parallel pixel processing and different pixel formats. These IP cores for programmable logic implementations are supplemented with AWB and AE software libraries that use video statistics data collected at the video inputs, software drivers, demo applications, reference SoC designs, and bit-accurate C-models.

[1]   *Included 3-month Xylon seat evaluation licenses for used Xylon logicBRICKS IP cores.*

Xylon's Automotive Video Camera

Packed in a compact, only a cubic inch big waterproof aluminum housing, Xylon's new automotive video camera provides excellent performance. Based on the Semiconductor® AR0231AT CMOS image sensor, the camera provides 30 Frames per Second (fps) of color 2.3 MP (1928x1280) video processed by an internal FPGA video processor. The FPGA integrates Xylon's complete logicBRICKS High Dynamic Range (HDR) Image Signal

Processing (ISP) pipeline. Cameras supplied with the logiISP-ZU-GMSL2 kit are equipped with the FIFO Optics miniature lens and short coax-cable leads with the Rosenberger FAKRA Z type connector.

Figure 3: Xylon logiCAM-GMSL2-AR0231 Video Camera

> **i**   To enable demonstration of multi-camera HDR ISP processing pipeline, cameras delivered with the kit output raw Bayer video. The cameras are Artix-7 FPGA-based and users can re-install the HDR ISP functionality and enable the color camera video with the provided firmware and initialization scripts.

The FPGA-based video cameras and the MPSoC-based logiISP-ZU-GMSL2 evaluation kit clearly demonstrate the flexibility of the HDR ISP processing pipeline, which is programmable logic-based and can be freely moved between the sensors and the main processing unit.

12-Ch Automotive Video FMC Card

The logiISP-ZU-GMSL2 kit comes with the logiFMC-GMSL2 video input FMC card. This add-on cards is designed primarily to enable quick prototyping and evaluation of automotive multi-camera Advanced Driver Assistance (ADAS) and Autonomous Driving (AD) applications, and it enables easy interfacing of up to twelve (12) automotive video cameras to hardware boards based on Xilinx's FPGA, SoC, MPSoC and ACAP video and vision processors.

Figure 4: Xylon's logiFMC-GMSL2 FMC Card

Related Design Services

Design services are available to customers interested in customization and enhancement developments based on the presented hardware and software products. For more information, please contact Xylon at info@logicbricks.com.

Related Xylon Products

The logiREF-MULTICAM-ISP reference demo design enables users to quickly adopt newly added multiplexing feature of logiISP and logiHDR IP cores. Multiplexing video channels through the same ISP (*Image Signal Processing*) pipeline saves significant amount of FPGA resources which, as a result, enables more channels to be processed on the same silicon. For more information, please visit out website:

　　Email:　　　support@logicbricks.com
　　URL:　　　　http://www.logicbricks.com/Products/logiREF-MULTICAM-ISP.aspx

Xylon's logiISP-UHD Image Signal Processing Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx's All Programmable devices. The logiISP-UHD ISP pipeline IP core can be supplemented with the logiHDR High Dynamic Range (HDR) Pipeline. To learn more, please visit our website:

　　URL:　　　　http://www.logicbricks.com/Products/logiISP.aspx

The logiHDR is an Ultra High Definition (UHD) HDR pipeline designed for digital processing and image quality enhancements of raw image data from HDR sensors. The logiHDR extracts maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by direct sunlight and objects placed in extreme shades:

　　URL:　　　　https://www.logicbricks.com/Products/logiHDR.aspx

Xylon provides software Auto White Balance (AWB) and Auto Exposure (AE) libraries for use with the logiISP-UHD IP core. To get more information about these products, please contact Xylon:

　　Email:　　　info@logicbricks.com

Ordering Information

Products are available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

　　Email:　　　sales@logicbricks.com
　　URL:　　　　http://www.logicbricks.com/Products/logiVID-ZU.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.

2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.00	18.05.2021	Initial release.
2.00	16.09.2021	Updated Figure 1 Avnet HDMI FMC card replaced with IP Core based solution for HDMI output.