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Features

- Full Xilinx® Spartan®-6 FPGA based design framework for:
  - Pedestrian Detection, and
  - Rear Looking Lane Departure Warning
- Development platform comes with preloaded demos and can be installed in test vehicles
- Reference FPGA designs with evaluation logicBRICKS™ IP cores
- SW drivers, APIs and post-processing libraries
- Calibration software for camera imager
- 25 hours of tech support (e-mail and phone)
- The platform includes:
  - Xilinx® Spartan®-6 SP605 Evaluation Kit with the XC6SLX45T-FGG484 FPGA
  - Xylon logiFMC-FPD-II FMC daughter card for 4 camera connections
  - DVI I/O FMC daughter card
  - OmniVision OV09715 1-megapixel camera with an active array size of 1280x800
  - Largan fish eye (wide FOV) 95321A lens
  - power supply and cabling

Figure 1: The logiPD-LDW Development Platform

Applications

Pedestrian Detection: Driving Assistance Systems, Video Surveillance, Robot Navigation, Assistive Technology for the Visually Impaired, Content Based Indexing, Advanced Human-Machine Interfaces, others

Rear Looking Lane Departure Warning System: Driving Assistance Systems

General Description

The logiPD-LDW Development Platform provides users with fundamental building blocks necessary to create two types of vision system applications based on the Xilinx Spartan-6 FPGA: the Pedestrian Detection and the Rear Looking Lane Departure Warning Systems. The demos require different system setups so only one demo can be running at a time.

Hardware, fully functional reference FPGA designs and associated software support provide users efficient means to fully assess the performance of logicBRICKS products in their own test platforms and targeted usage conditions, i.e. driving conditions in case of automotive applications. Functions incorporated in the logiPD-LDW development platform can save months of development time.

The logiPD-LDW offers a complete FPGA based engine capable to detect pedestrians/humans using a video image from a camera (Figure 2). Its application fields range from video surveillance, driving assistance systems, robot navigation, assistive technology for the visually impaired, content-based indexing to advanced human-machine interfaces and other applications.

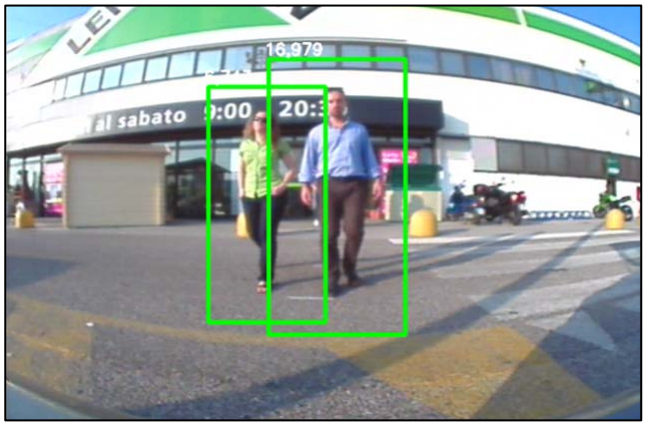

Figure 2: The Pedestrian Screenshot

Lane Departure Warning Systems (LDWS) are typically electronic automotive systems that indentify and track the markings corresponding to the lane boundaries, locate the vehicle position with respect to them and issue a warning when the vehicle crosses the lane bounds. Typically the LDWS systems are forward looking and use a camera(s) mounted in front of a vehicle. The logiPD-LDW platform demonstrates the Rear Looking Lane Departure Warning system that offers many advantages: work with a camera mounted at the back-end of the vehicle, simpler, robust and fast to compute lane model. The back-end mounted cameras are typically used for Rear-View Camera application, Surround View, etc., which means that the Rear Looking LDWS can be added in the FPGA based automotive system with no additional costs in regard to vision sensors.

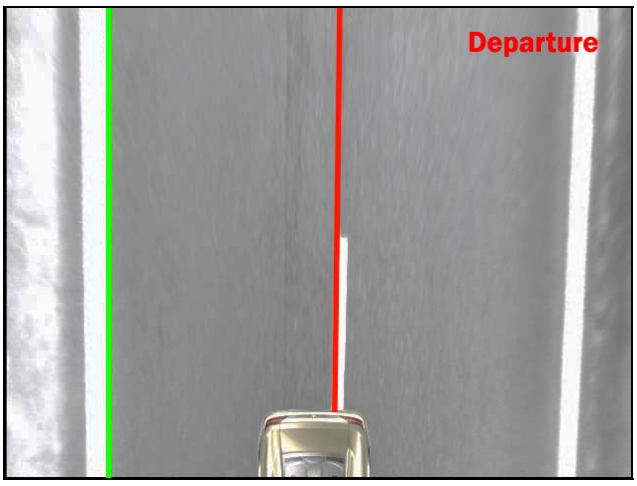

Figure 3: Departure Warning logiPD-LDW Screenshot

Both demo applications can run with a camera input, as presented by Figure 4.

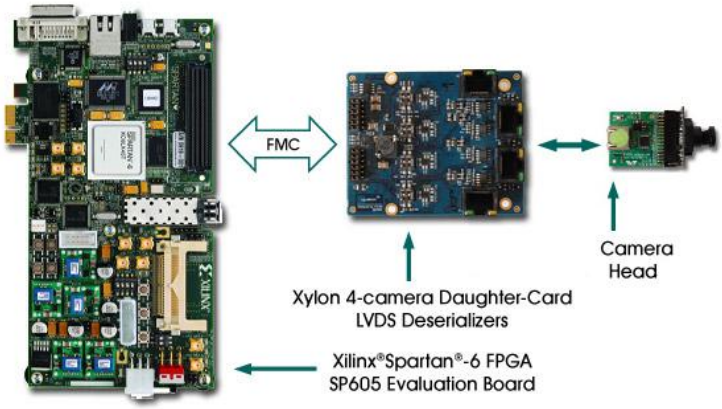

Figure 4: logiPD-LDW Setup with the Camera

In a configuration with the DVI I/O FMC module (Figure 5), the development system enables lab work with movies taken from a real vehicle in different driving conditions. This setup currently supports the Rear Looking Lane Departure Warning demo only.

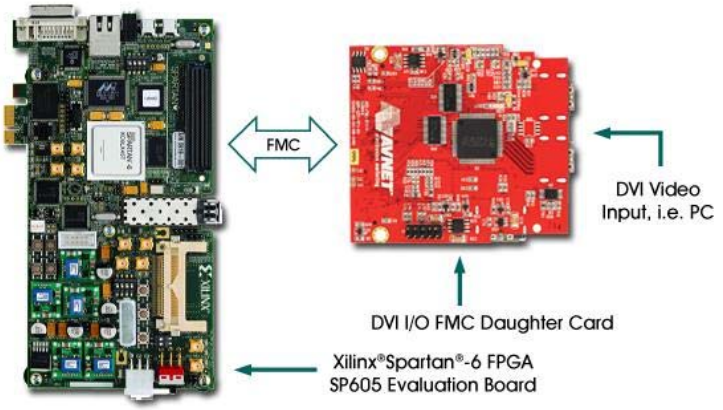

Figure 5: logiPD-LDW Setup with the DVI I/O FMC

logicBRICKS IP Cores

The key elements of this development platform are logicBRICKS IP cores designed and optimized for use in Xilinx programmable devices. The provided software support includes application examples, drivers, APIs, post-processing library and calibration software. Reference designs provided with the platform are implemented with evaluation logicBRICKS IP cores.

Find more information about logicBRICKS evaluation IP cores by visiting:
http://www.logicbricks.com/logicBRICKS/Evaluation-logicBRICKS.aspx

logiPDET Pedestrian Detector

This is an HOG/SVM-based pedestrian detection IP core developed for vision-based embedded applications. The algorithm follows a discriminative approach. It combines a HOG-based descriptor and a SVM classier. The HOG (Histogram of Oriented Gradients) is a descriptor designed to encode pedestrian structure. The SVM (Support Vector Machine) is a non probabilistic binary linear classifier trained to recognize pedestrian's size.

Find more information by visiting http://www.logicbricks.com/Products/logiPDET.aspx.

logiLMD Lane Marking Detector

This IP core detects the lane markings on the roadway captured from a rear view camera. Its functions include image-processing filters, like Gaussian smoothing and Edge detection, and blocks specifically tailored for lane marking detections. The output of the core is a set of straight lines corresponding to the lane markings.

Find more information by visiting http://www.logicbricks.com/Products/logiLMD.aspx.

logiVIEW Perspective Transformation and Lens Correction Image processor

The logiVIEW IP core is the key IP core for the design of the Surround View and similar multi-camera systems. This IP core removes fish eye lens distortions, makes perspective corrections to all camera video inputs and stitches the resulting single image in real-time. A programmable homographic transformation matrix enables different perspective transformations, such as rotating, resizing, translating, cropping, as well as simultaneous combinations of all of these transformations. When configured to use Memory Look-Up Tables (MLUT), the logiVIEW can make any nonlinear transformation.

Find more information by visiting www.logicbricks.com/Products/logiVIEW.aspx.

logiWIN Versatile Video Input

The logiWIN IP core accepts a streaming video input, decodes it and converts into the RGB format. The input video can be real-time scaled, de-interlaced, cropped and positioned on the video display. The logiWIN integrates high-quality anti-aliasing algorithm that guarantees high picture quality without visible artifacts.

Find more information by visiting www.logicbricks.com/Products/logiWIN.aspx.

logiBAYER Color Camera Sensor Bayer Decoder

Today most common single-chip cameras use CMOS sensors with pixels arranged in Bayer color pattern. Bayer filter in front of the sensor embeds color information into sensor's pixels and each pixel is an actual monochrome color element. The CMOS sensor's output must be converted into a human-viewable picture by conversion from the Bayer image to an RGB image.

Find more information by visiting www.logicbricks.com/Products/logiBAYER.aspx.

logiCVC-ML Compact Multilayer Video Controller

The logiCVC-ML IP core is an advanced display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems with Xilinx Zynq-7000 EPP and FPGAs. This IP core is the cornerstone of all 2D and 3D GPUs. Though it's main function is to provide flexible display control, with resolutions up to 2048x2048 pixels, it also includes a level of hardware acceleration: alpha blendings, panning, buffering of multiple frames, etc.

Find more information by visiting www.logicbricks.com/Products/logiCVC-ML.aspx.

Package Content

Hardware

- 1x Xilinx Spartan-6 FPGA SP605 Evaluation kit (Spartan-6 XC6SLX45T-FGG484)
- 1x Xylon logiFMC-FPD-II FMC daughter card
- 1x DVI I/O FMC daughter card
- 1x Omnivision OV09715 1-megapixel camera sensor
- 1x Largan fish eye (wide FOV) 95321A lens
- 1x National Semiconductor® FPD-Link II serializer board for camera sensor

Reference FPGA Designs

Designs are compatible with the Xilinx Platform Studio implementation tool.

- Pedestrian detection demo design
- Rear Looking Lane Departure Warning + camera input demo design
- Rear Looking Lane Departure Warning + DVI video input demo design

logicBRICKS IP Cores*

- logiPDET Pedestrian Detector
- logiLMD Lane Marking Detector
- logiVIEW Perspective Transformation and Lens Correction Image processor
- logiWIN Versatile Video Input
- logiBAYER Color Camera Sensor Bayer Decoder
- logiCVC-ML Compact Multilayer Video Controller

* Xylon provides the evaluation IP cores with the kit

Applications and Drivers

- Pedestrian detection application
- Rear Looking LDW application
- Calibration software for Lens and Vehicle calibration

Documentation

- Demo User's Manuals
- logicBRICKS User's Manuals
- SW manuals

Cabling and Adapters

- power supply
- cabling

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Xilinx system Generator for DSP (MathWorks Matlab/Simulink) to source model access
- C programming

The logicBRICKS IP cores are fully supported by the Xilinx Platform Studio and the EDK, and their use does not require any particular skills beyond general Xilinx tools knowledge.

Xylon Design Services

Xylon provides design services to customers who want to refine reference design performance to meet their particular application.

Related Xylon Products

To learn more about the logicBRICKS IP cores used in this design:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/IP-Cores.aspx

To learn more about the logiFMC-FPD-II FMC daughter card supporting the National FPD-Link II (Flat Panel Display Link) serial interface:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiFMC-FPD-II.aspx

Ordering Information

This product is available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiPD-LDW.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00	10.05.2012	Initial datasheet release.

The logiPDET and the logiLMD cores are sourced from Technology Partner eVS embedded Vision Systems Srl.