Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	Data Sheet
Design File Formats	Encrypted VHDL VHDL sources available at extra cost
Constraints Files	Reference design ucf
Reference Designs & Application Notes	Reference designs available for Xilinx ZC702/ZC706 development kits and the ZedBoard™ kit from Avnet Electronics Marketing
Additional Items	Software drivers for different OS
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Graphics Accelerator IP designed to support the OpenGL® ES 1.1 API* (Common Profile)
- Supports Xilinx® Zynq®-7000 AP SoC, 6 and 7 series Xilinx All Programmable FPGAs
- Conformant to the AMBA® AXI4 bus specifications from ARM®
- Linux, WCE and Android compatible
- FPGA resource-effective 3D acceleration
- ARM Cortex™-A9 CPU Core with NEON™ runs the geometry engine and optimizes the IP's size
- The logi3D can be used with different CPUs
- Hardware implemented 3D graphics algorithms:
  - Occlusion culling
  - Gouraud shading
  - MIP-MAP level of the texture per pixel
  - Texture filtering: point sampling, bilinear filtering and trilinear filtering
  - Fog function per vertex
  - Alpha Blending
  - Full Screen Anti-aliasing

**Product is based on a published Khronos Specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.*

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) clk	LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
ZYNQ®-7 (XC7Z020-1)	100	48448	7570 (14325/25539)	0	0	14	38	0	N/A	Vivado 2018.3
ZYNQ®-7 (XC7Z045-2)	170	49319	7706 (14334/25540)	0	0	14	38	0	N/A	Vivado 2018.3
Kintex®-7 (XC7K325T-2)[3]	170	43840	6850 (12306/21411)	0	0	5	29	0	N/A	Vivado 2014.3

Notes:
1) Assuming 64-bit AMBA AXI4 memory interfaces, readable registers, enabled bilinear interpolation, texture mipmap and alpha blending
2) Assuming memory interfaces are connected internally
3) Texture mimpam feature not implemented

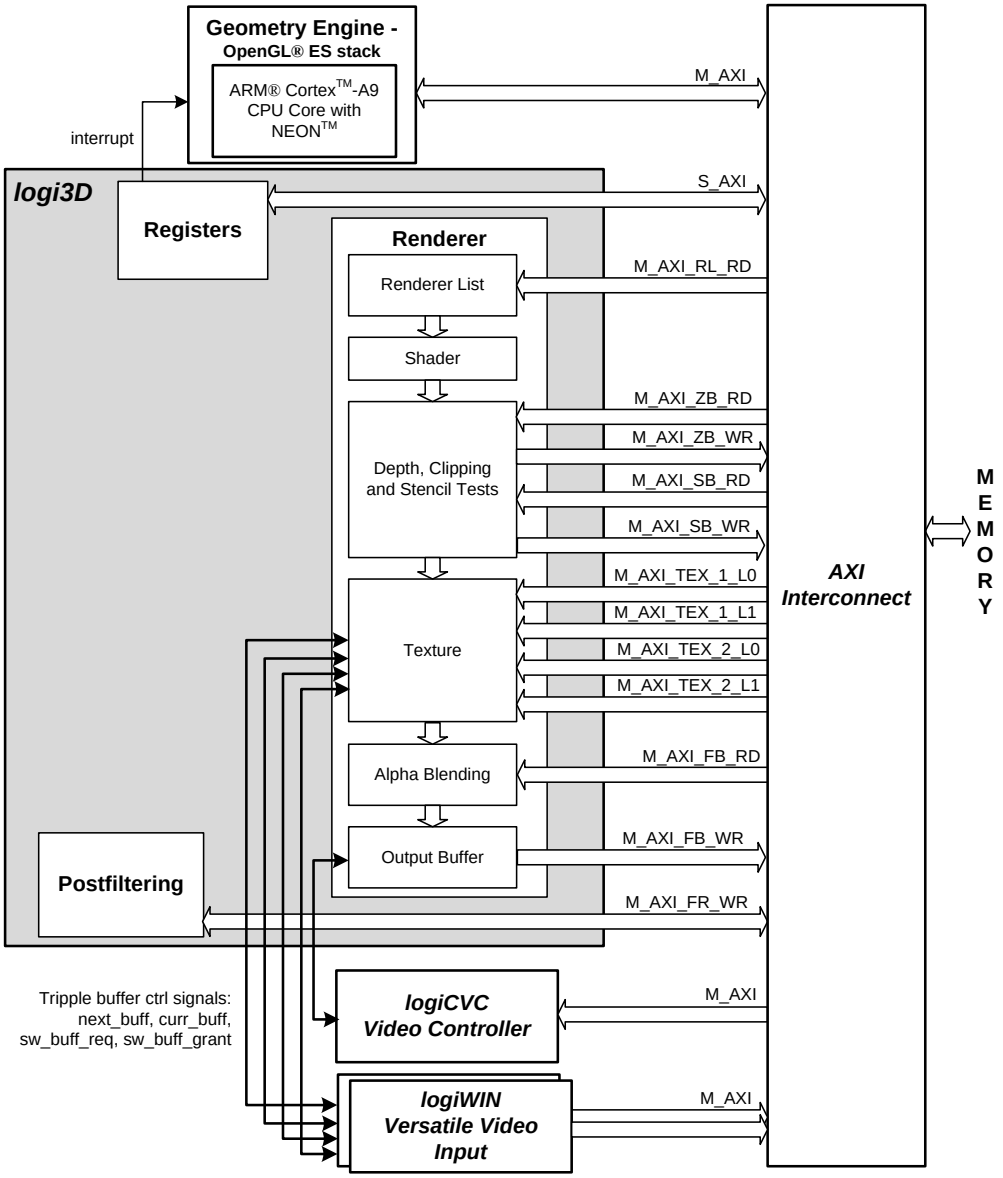

Figure 1: logi3D Architecture

Features (cont)

- Prepared for Xilinx Vivado® Design Suite (IP Integrator) and ISE® Design Suite (XPS)
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Available free reference designs for the most popular Zynq-7000 AP SoC based development kits
- Plug-and-Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiCVC-ML Compact Multilayer Video Controller and logiBITBLT Bit Block 2D Graphics Accelerator

Applications

The logi3D Scalable 3D Graphics Accelerator can be used as a graphics processing unit (GPU) in graphics applications requiring high-performance and attractive graphics effects, such as scalable user interfaces, visualizations, navigation, automotive, etc. The IP core is especially suited for use in Xilinx Zynq-7000 AP SoC which combine the power of an industry–standard ARM Cortex-A9 MPCore™ processing system with custom designed IP cores implemented in programmable logic available on the same chip.

General Description

The logi3D Scalable 3D Graphics Accelerator IP core is specifically designed for the Xilinx Zynq-7000 All Programmable (AP) SoC. The logi3D enables designers to add attractive 2D and 3D graphics, including advanced Graphical User Interfaces (GUI), to their Xilinx Zynq-7000 AP System-On-Chip (SoC). This high performing 3D graphics processing unit (GPU) can be implemented with other soft IP cores in Zynq-7000 AP SoC programmable logic and interfaced with an industry-standard ARM dual-core Cortex-A9 MPCore™ processing system available on the same chip. Due to its AMBA AXI4 compliance the logi3D IP core can also be implemented in Xilinx 7-series and other Xilinx FPGA families as a graphics coprocessor in various ASSP plus FPGA combinations.

The logi3D Scalable 3D Graphics Accelerator IP core is designed to support the OpenGL ES 1.1 API. Linux, Microsoft® Windows® Embedded Compact and Android are the currently supported operating systems. The current firmware works with the ARM processors and can be re-compiled for different CPUs. The assembly code acceleration can be used with ARM processors supported by the ARM NEON coprocessor. As a part of IP deliverables, Xylon also provides demo application that uses simple Xylon's 3D engine (3DS format supported).

The logi3D Scalable 3D Graphics Accelerator IP core is designed from the ground up for the most efficient Xilinx Zynq-7000 AP SoC implementations. The IP is carefully partitioned between hardware and software to assure the highest performances and optimal utilization of FPGA resources, i.e. the complex geometry engine uses the ARM NEON coprocessor programmed in the optimized assembly code, while the rendering engine works fully in the on-chip programmable logic. Special care has been taken to assure a lot of free programmable logic resources for other IP cores used alongside the logi3D IP core in the same Xilinx Zynq-7000 AP SoC. The programmability of programmable logic allows for future extensions of the logi3D functionality and the design of graphics solutions customized at the hardware and software level.

The logi3D is a parametrizable and scalable Graphics Processing Unit (GPU) IP core that allows advanced and highly customized graphic controller designs. The logi3D IP core is fully embedded into Xilinx Vivado IP Integrator and ISE Xilinx Platform Studio implementation tools, and its integration with the on-chip AXI4 bus is very simple. Designers can setup the IP core through a GUI, optimize feature sets and control the utilization of programmable logic and implement the complete Xilinx SoC in a drag & drop fashion. This scalable approach enables an exact match of customer requirements and enabled IP features. Customers set up exact systems' performance level and pay only for what they need. The logi3D can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores for building of advanced GUI embedded systems.

Functional Description

Figure 1 presents the logi3D block diagram. The main logi3D functional blocks are: Geometry Engine, Rasterizer, Post-filtering and Registers.

Geometry Engine

The Geometry Engine is a complex 3D engine's stage that executes per-polygon and per-vertex operations and complex math operations. Its sub-stages can be generally nominated as: model view, lighting, projection, clipping and screen mapping. A pure HW implementation of the geometry stage would be too costly within the FPGA from the slice consumption point of view. The logi3D IP core's geometry stage is carefully HW/SW partitioned for optimum execution speed and FPGA slice consumption. A majority of necessary 3D transformations are executed by a dedicated ARM Cortex-A9 CPU Core with the NEON coprocessor. Processor data and instruction memories are implemented in the common SDRAM-type memory used for logi3D operations.

Rasterizing

The rasterizer stage does per-pixel operations. It resolves the pixel elements' colors by means of the colour-buffer with an associated Alpha channel. The Rasterizer checks visibility of various objects (occlusion culling) within the 3D scene and resolves it by a mean of the Z-buffer. The 3D scene's realism is further increased by texturing that actually "glues" images onto 3D objects. The logi3D IP core enables various modes of texture operations especially tailored for Xilinx FPGA operations. The fastest texturing is achieved by way of a 2-way

texture cache that fits into Xilinx on-chip Block RAM memory modules. In addition, the logi3D enables the storage of textures within the common memory, as well as mip-mapping. For memory accesses the Rasterizer uses AMBA AXI4 which assures high data throughput and allows for easy system integrations. The logi3D IP core implements triple buffering to enable the fastest artifact-free rendering in the on-screen memory, as well as artifact-free live video texturing.

Post-filtering

This final stage enables 4X fully rendered 3D scene's anti-aliasing. Post-filtering outputs the final 3D graphics picture prepared for display. The picture must be sent to display(s) via dedicated video controller(s), such as the logiCVC-ML Compact Multilayer Video Controller from Xylon's logicBRICKS IP library.

Core Modifications

The core is supplied in encrypted VHDL formats compatible with Xilinx Vivado IP Integrator and ISE Xilinx Platform Studio implementation tools. Many logi3D configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logi3D VHDL Configuration Parameters

Parameter	Description
C_XY_LENGTH	Maximal horizontal and vertical position coordinates
C_USE_BILINEAR	Use bilinear interpolation
C_USE_MIPMAP	Use texture mip-maping
C_USE_MULTITEXTURE	Use 2nd texture unit
C_USE_AA	Use anti-aliasing
C_USE_ALPHA_BLEND	Use alpha blending
C_USE_STENCIL	Use stencil buffer

The OpenGL ES 1.1 implementation is optimally shared between software and hardware. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logi3D core, or to supplement some of your specific functions, you can order the source code or allow us to tailor the logi3D graphics processing unit to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous set/reset
MEM_CLK	Input	Clock port for XMB memory interfaces
Memory Interface		
S_AXI interface	Bus	Slave AXI interface. Refer to AXI interface specification
M_AXI interface CH0	Bus	Master AXI interface channel 0. Refer to AXI interface specification
M_AXI interface CH1	Bus	Master AXI interface channel 1. Refer to AXI interface specification
M_AXI interface CH2	Bus	Master AXI interface channel 2. Refer to AXI interface specification

Signal	Signal Direction	Description
M_AXI interface CH3	Bus	Master AXI interface channel 3. Refer to AXI interface specification
M_AXI interface CH4	Bus	Master AXI interface channel 4. Refer to AXI interface specification
M_AXI interface CH5	Bus	Master AXI interface channel 5. Refer to AXI interface specification
M_AXI interface CH6	Bus	Master AXI interface channel 6. Refer to AXI interface specification
M_AXI interface CH7	Bus	Master AXI interface channel 7. Refer to AXI interface specification
M_AXI interface CH8	Bus	Master AXI interface channel 8. Refer to AXI interface specification
M_AXI interface CH9	Bus	Master AXI interface channel 9. Refer to AXI interface specification
M_AXI interface CH10	Bus	Master AXI interface channel 10. Refer to AXI interface specification
M_AXI interface CH11	Bus	Master AXI interface channel 11. Refer to AXI interface specification
XMB interface CH0	Bus	XMB interface channel 0. Refer to logiMEM User's Manual
XMB interface CH1	Bus	XMB interface channel 1. Refer to logiMEM User's Manual
XMB interface CH2	Bus	XMB interface channel 2. Refer to logiMEM User's Manual
XMB interface CH3	Bus	XMB interface channel 3. Refer to logiMEM User's Manual
XMB interface CH4	Bus	XMB interface channel 4. Refer to logiMEM User's Manual
XMB interface CH5	Bus	XMB interface channel 5. Refer to logiMEM User's Manual
XMB interface CH6	Bus	XMB interface channel 6. Refer to logiMEM User's Manual
XMB interface CH7	Bus	XMB interface channel 7. Refer to logiMEM User's Manual
XMB interface CH8	Bus	XMB interface channel 8. Refer to logiMEM User's Manual
XMB interface CH9	Bus	XMB interface channel 9. Refer to logiMEM User's Manual
XMB interface CH10	Bus	XMB interface channel 10. Refer to logiMEM User's Manual
XMB interface CH11	Bus	XMB interface channel 11. Refer to logiMEM User's Manual
Auxiliary Signals		
CURR_VBUFF(1:0)	Output	Triple buffering: Current video memory buffer
NEXT_VBUFF(1:0)	Input	Triple buffering: Next video memory buffer to write to
SW_VBUFF_REQ	Output	Triple buffering: Request for buffer switching
SW_VBUFF_GRANT	Input	Triple buffering: Buffer switching granted
TEX_1_L0_CURR_BUF(1:0)	Input	Texture 1 mipmap level 0 triple buffering: Current video memory buffer
TEX_1_L0_NEXT_BUF(1:0)	Output	Texture 1 mipmap level 0 triple buffering: Next video memory buffer to write to
TEX_1_L0_SW_BUF_REQ	Input	Texture 1 mipmap level 0 triple buffering: Request for buffer switching
TEX_1_L0_SW_BUF_GRANT	Output	Texture 1 mipmap level 0 triple buffering: Buffer switching granted
TEX_1_L1_CURR_BUF(1:0)	Input	Texture 1 mipmap level 1 triple buffering: Current video memory buffer
TEX_1_L1_NEXT_BUF(1:0)	Output	Texture 1 mipmap level 1 triple buffering: Next video memory buffer to write to
TEX_1_L1_SW_BUF_REQ	Input	Texture 1 mipmap level 1 triple buffering: Request for buffer switching
TEX_1_L1_SW_BUF_GRANT	Output	Texture 1 mipmap level 1 triple buffering: Buffer switching granted
TEX_2_L0_CURR_BUF(1:0)	Input	Texture 2 mipmap level 0 triple buffering: Current video memory buffer
TEX_2_L0_NEXT_BUF(1:0)	Output	Texture 2 mipmap level 0 triple buffering: Next video memory buffer to write to
TEX_2_L0_SW_BUF_REQ	Input	Texture 2 mipmap level 0 triple buffering: Request for buffer switching
TEX_2_L0_SW_BUF_GRANT	Output	Texture 2 mipmap level 0 triple buffering: Buffer switching granted
TEX_2_L1_CURR_BUF(1:0)	Input	Texture 2 mipmap level 1 triple buffering: Current video memory buffer
TEX_2_L1_NEXT_BUF(1:0)	Output	Texture 2 mipmap level 1 triple buffering: Next video memory buffer to write to
TEX_2_L1_SW_BUF_REQ	Input	Texture 2 mipmap level 1 triple buffering: Request for buffer switching
TEX_2_L1_SW_BUF_GRANT	Output	Texture 2 mipmap level 1 triple buffering: Buffer switching granted
INTERRUPT	Output	logi3D interrupt signal, level sensitive, high active
TRIANGLE_END	Output	Triangle end

Verification Methods

The logi3D is checked against conformance tests and fully supported by the Xilinx Vivado and ISE Design Suites. This tight integration tremendously shortens IP integration and verification. A full logi3D implementation does not require any particular skills beyond general Xilinx tools knowledge. The encrypted IP is shipped with the reference design and compiled simulation libraries for the ModelSim. The logi3D evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logi3D.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon provides free pre-verified reference designs to showcase the logi3D graphics accelerator, other Xylon's logicBRICKS 2D graphics accelerators and the display controller on the most popular Xilinx Zynq-7000 AP SoC based development kits. Reference designs include evaluation logicBRICKS IP cores and hardware design files, OS image, software drivers, demo applications and documentation. To check a full list of Xylon reference designs please visit the web:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

logiREF-ZGPU-ZC702 Reference Design – evaluate 2D and 3D logicBRICKS graphics on Xilinx ZC702 Evaluation Board with connected PC monitor. Deliverables include complete software support for Linux OS, from the basic FrameBuffer up to the full OpenGL ES 1.1 API. Configurable IP cores enable customization of the evaluation hardware, which can be also used with other popular operating systems.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000.aspx

logiREF-ZGPU-ZC706 Reference Design – Functionally equal to the logiREF-ZGPU-ZC702 reference design, but prepared for the powerful Xilinx ZC706 Evaluation Board:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000-ZC706.aspx

logiREF-ZGPU-ZED Reference Design is functionally equal to the logiREF-ZGPU-ZC702 reference design – showcases the full 2D and 3D graphics engine running on the ZedBoard development kit from Avnet Electronics Marketing.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Zynq-AP-SoC-ZedBoard.aspx

To learn more about the available software support for the logi3D 3D Graphics Accelerator IP core, please contact Xylon or visit our web site:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.01.	20.10.2010	Initial Xylon release – new doc template
1.02	06.07.2011	First IP release with the Xilinx Zynq-7000 and 7-series FPGA support
1.03	10.10.2011	ARM AMBA AXI4 bus compliant version
1.04	10.10.2012	Added ZYNQ Table 1 updated Figure 1 updated Table 3 updated
1.05	02.01.2014.	Vivado Design Suite compatible version Data sheet document corrections Table 3. updated
1.5	18.11.2014.	Document updated with information about the Xilinx Vivado compatible logi3D IP core. New versioning scheme introduced for Vivado

Version	Date	Note
		packaged IP core.
	12.04.2019.	Updated Table 1.