



### Xylon d.o.o.

Fallerovo setaliste 22  
10000 Zagreb, Croatia  
Phone: +385 1 368 00 26  
Fax: +385 1 365 51 67  
E-mail: [info@logicbricks.com](mailto:info@logicbricks.com)  
URL: [www.logicbricks.com](http://www.logicbricks.com)

### Features

- Available under terms of the SignOnce IP License
- Digital FM modulator for IR audio broadcast standard
- Supports standard FM carrier frequencies (2.3 MHz, 2.8 MHz, 3.2 MHz, 3.8 MHz)
- Configurable as stereo or mono IR audio FM modulator
- Accentuation of higher frequencies band through an optional digital filter
- Supports different sampling rates of streaming audio (22 kHz, 32 kHz, 44.1 kHz, 96 kHz, 192 kHz)
- Supports all sample resolutions of streaming audio
- Frequency deviation +/- 75 kHz
- Optimized for low slice count
- Parametrizable VHDL design that allows customization and tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK

<b>Core Facts</b>	
<b>Provided with Core</b>	
Documentation	User Manual
Design File Formats	Encrypted VHDL
Constraints Files	logiair.ucf
Verification	VHDL Test Bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	EDK sample design
Additional Items	Xylon logiCRAFT2 and logiCRAFT3 Evaluation Boards
<b>Simulation Tool Used</b>	
ModelTech's Modelsim	
<b>Support</b>	
Support Provided by Xylon	

**Table 1: Example Implementation Statistics for Xilinx® FPGAs**

Family	Example Device	Fmax (MHz)	Slices <sup>1</sup>	IOB <sup>2</sup>	GCLK	BRAM	MULT/DSP48/E	DCM / CMT	MGT	Design Tools
Spartan®-3	XC3S1000-5	50	658	37	1	0	0	0	N/A	ISE® 10.1.03i
Automotive Spartan®-3E	XA3S1200E-4	50	658	37	1	0	0	0	N/A	ISE® 10.1.03i
Virtex®-II Pro	XC2VP4-7	66	657	37	1	0	0	0	N/A	ISE® 10.1.03i
Virtex®-4	XC4VFX12-12	76	652	37	1	0	0	0	N/A	ISE® 10.1.03i
Virtex®-5	XC5VLX30-3	96	319	37	1	0	0	0	N/A	ISE® 10.1.03i

Notes:

- 1) Assuming stereo audio channel, 16-bit audio sample, 44.1kHz sampling rate, included EQ-filter for accentuation
- 2) Assuming all core I/Os and clocks are routed off-chip

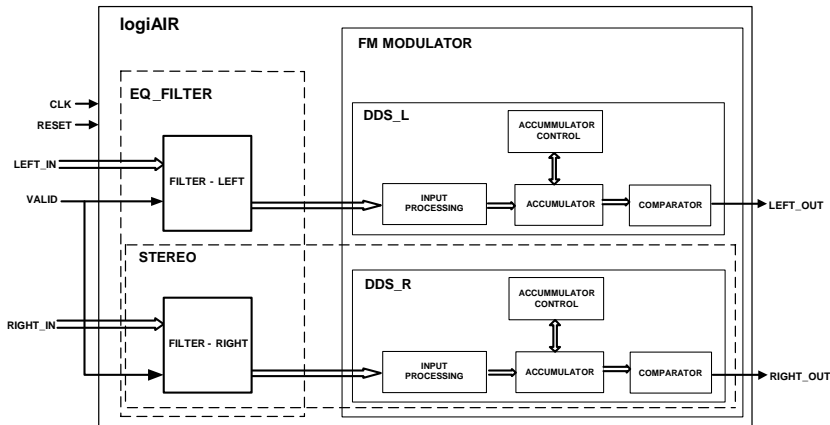


Figure 1: logiAIR Block Diagram

## Applications

- Car Infotainment
- Home Infotainment

## General Description

The logiAIR core – Audio IR digital FM modulator enables wireless transmission of audio signal through an infrared link. The core modulates digital audio signals onto selected carrier frequencies by using FM technique. Modulated FM signal is fed to the simple IR emitter. The emitter converts the modulated signal into infrared light detected by headphones' receivers.

The emitter's components (transistor, diode, and LEDs) must be able to operate on carrier frequencies, and with selected IR emission wavelength. Headphones' receiver decodes the infrared signal, demodulates it, and filters it to an audio frequency range from 20 Hz to 20 KHz. The Headphones deliver clear stereo sound.

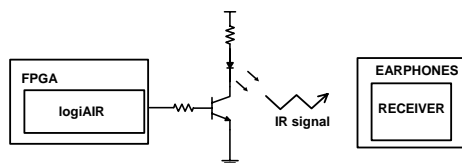


Figure 2: Audio Infrared Link featuring the logiAIR

The logiAIR IP core supports audio signals with various sample resolutions and sampling rate frequencies. Input sync signals synchronize input audio streams with internal core's logic. The logiAIR modulates audio signal onto standard carrier frequency pairs (2.3 MHz and 2.8 MHz called Channel A; 3.2 MHz and 3.8 MHz called Channel B), and with the standard frequency deviation of +/- 75 KHz. Its output is in compliance with all standard IR headphones. Carrier frequencies are generated from the main clock signal frequency during synthesis, by mean of a simple core parameters' setting.

## Functional Description

The logiAIR's uses Direct Digital Synthesis (DDS) module to create modulated signal in a form of binary pulse train fed into emitters. The DDS module consists of few submodules: Accentuation Filter, Input Registers, Accumulator with Control Logic, and Output Comparator.

### Accentuation Filter

This optional filter accentuates high band frequencies prior to the FM modulation. The filter improves the signal/noise ratio. Its coefficients are automatically set in accordance to inputs sampling rates.

### Input Processor

This sub module contains input registers used to capture audio bit stream synchronized with data valid signal. Offset value is added to audio signal to setup correct modulating frequency.

### Accumulator & Control Logic

Accumulator is limited with calculated overflow value to be able to work on desired carrier frequency without discontinuity. Control logic detects overflow state and assures correct value in the accumulator.

### Output Comparator

Output comparator compares accumulator's value to a calculated value for the carrier frequency. Generated registered binary pulse trains are inputs to LED drivers.

## Core Modifications

The core is supplied in an encrypted VHDL format and a number of configuration parameters are selectable prior to VHDL synthesis.

**Table 2: logiSTEP Parameters**

Parameter	Description
CLK_FREQ	Clock frequency
AUDIO_BIT	Audio sample data width
STEREO	Mono or stereo mode
EQ_FILTER	Include equalization filter
CARRIERS	FM carriers frequency
SAMPLE_RATE	Audio sample rate

## Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 3.

**Table 3: Core I/O Signals.**

Signal	Signal Direction	Description
LEFT_IN[AUDIO_BIT-1:0]	Input	Left mono channel audio stream
RIGHT_IN[AUDIO_BIT-1:0]	Input	Right mono channel audio stream
VALID	Input	Data valid
RESET	Input	Reset
CLK	Input	Clock
LEFT_OUT	Output	Left channel FM modulated signal (mono channel)
RIGHT_OUT	Output	Right channel FM modulated signal (mono channel)

## Verification Methods

The logiAIR is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiAIR implementation does not require any particular skills beyond general Xilinx tools knowledge.

## Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

## Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on logiCRAFT2 and logiCRAFT3 Xylon development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. Both platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. The platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: [info@logicbricks.com](mailto:info@logicbricks.com)

URL: [www.logicbricks.com/html/evaluation\\_boards.htm](http://www.logicbricks.com/html/evaluation_boards.htm)

## Ordering Information

This product is available directly from Xylon under the terms of the SignOnce IP License. Please contact Xylon for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Xylon or visit the web:

Email: [commonlicense@xilinx.com](mailto:commonlicense@xilinx.com)

URL: [www.xilinx.com/ipcenter/signonce](http://www.xilinx.com/ipcenter/signonce)

This publication has been carefully checked for accuracy. However, Xylon does not assume any responsibility for the contents or use of any product described herein. Xylon reserves the right to make any changes to product without further notice. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. Xylon products are not intended for use in the life support applications. Use of the Xylon products in such appliances is prohibited without written Xylon approval.

## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.

2100 Logic Drive

San Jose, CA 95124

Phone: +1 408-559-7778

Fax: +1 408-559-7114

URL: [www.xilinx.com](http://www.xilinx.com)

## Revision History

Version	Date	Note
1.00.	03.03.2009	New doc template