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Features

- Available under terms of the SignOnce IP License
- Digital FM modulator for IR audio broadcast standard
- Supports standard FM carrier frequencies (2.3 MHz, 2.8 MHz, 3.2 MHz, 3.8 MHz)
- Configurable as stereo or mono IR audio FM modulator
- Accentuation of higher frequencies band through an optional digital filter
- Supports different sampling rates of streaming audio (22 kHz, 32 kHz, 44.1 kHz, 96 kHz, 192 kHz)
- Supports all sample resolutions of streaming audio
- Frequency deviation +/- 75 kHz
- Optimized for low slice count
- Parametrizable VHDL design that allows customization and tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK

Table 1: Example Implementation Statistics for Xilinx® FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Slices</th>
<th>IOB</th>
<th>GCLK</th>
<th>BRAM</th>
<th>MULTI/ DSP48/E</th>
<th>DCM / CMT</th>
<th>MGT</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan®-3</td>
<td>XC3S1000-5</td>
<td>50</td>
<td>658</td>
<td>37</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>Automotive</td>
<td>XA3S1200E-4</td>
<td>50</td>
<td>658</td>
<td>37</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>Spartan®-3E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex®-II Pro</td>
<td>XC2VP4-7</td>
<td>66</td>
<td>657</td>
<td>37</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>Virtex®-4</td>
<td>XC4VF12-12</td>
<td>76</td>
<td>652</td>
<td>37</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>Virtex®-5</td>
<td>XC5VLX30-3</td>
<td>96</td>
<td>319</td>
<td>37</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Notes:
1) Assuming stereo audio channel, 16-bit audio sample, 44.1kHz sampling rate, included EQ-filter for accentuation
2) Assuming all core I/Os and clocks are routed off-chip
Applications
• Car Infotainment
• Home Infotainment

General Description
The logiAIR core – Audio IR digital FM modulator enables wireless transmission of audio signal through an infrared link. The core modulates digital audio signals onto selected carrier frequencies by using FM technique. Modulated FM signal is fed to the simple IR emitter. The emitter converts the modulated signal into infrared light detected by headphones’ receivers.

The emitter’s components (transistor, diode, and LEDs) must be able to operate on carrier frequencies, and with selected IR emission wavelength. Headphones’ receiver decodes the infrared signal, demodulates it, and filters it to an audio frequency range from 20 Hz to 20 KHz. The Headphones deliver clear stereo sound.

Functional Description
The logiAIR’s uses Direct Digital Synthesis (DDS) module to create modulated signal in a form of binary pulse train fed into emitters. The DDS module consists of few submodules: Accentuation Filter, Input Registers, Accumulator with Control Logic, and Output Comparator.
Accentuation Filter
This optional filter accentuates high band frequencies prior to the FM modulation. The filter improves the signal/noise ratio. Its coefficients are automatically set in accordance to inputs sampling rates.

Input Processor
This sub module contains input registers used to capture audio bit stream synchronized with data valid signal. Offset value is added to audio signal to setup correct modulating frequency.

Accumulator & Control Logic
Accumulator is limited with calculated overflow value to be able to work on desired carrier frequency without discontinuity. Control logic detects overflow state and assures correct value in the accumulator.

Output Comparator
Output comparator compares accumulator’s value to a calculated value for the carrier frequency. Generated registered binary pulse trains are inputs to LED drivers.

Core Modifications
The core is supplied in an encrypted VHDL format and a number of configuration parameters are selectable prior to VHDL synthesis.

Table 2: logiSTEP Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_FREQ</td>
<td>Clock frequency</td>
</tr>
<tr>
<td>AUDIO_BIT</td>
<td>Audio sample data width</td>
</tr>
<tr>
<td>STEREO</td>
<td>Mono or stereo mode</td>
</tr>
<tr>
<td>EQ_FILTER</td>
<td>Include equalization filter</td>
</tr>
<tr>
<td>CARRIERS</td>
<td>FM carriers frequency</td>
</tr>
<tr>
<td>SAMPLE_RATE</td>
<td>Audio sample rate</td>
</tr>
</tbody>
</table>

Core I/O Signals
The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 3.

Table 3: Core I/O Signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Signal Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEFT_IN[AUDIO_BIT-1:0]</td>
<td>Input</td>
<td>Left mono channel audio stream</td>
</tr>
<tr>
<td>RIGHT_IN[AUDIO_BIT-1:0]</td>
<td>Input</td>
<td>Right mono channel audio stream</td>
</tr>
<tr>
<td>VALID</td>
<td>Input</td>
<td>Data valid</td>
</tr>
<tr>
<td>RESET</td>
<td>Input</td>
<td>Reset</td>
</tr>
<tr>
<td>CLK</td>
<td>Input</td>
<td>Clock</td>
</tr>
<tr>
<td>LEFT_OUT</td>
<td>Output</td>
<td>Left channel FM modulated signal (mono channel)</td>
</tr>
<tr>
<td>RIGHT_OUT</td>
<td>Output</td>
<td>Right channel FM modulated signal (mono channel)</td>
</tr>
</tbody>
</table>

Verification Methods
The logiAIR is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiAIR implementation does not require any particular skills beyond general Xilinx tools knowledge.
Recommended Design Experience

The user should have experience in the following areas:
- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKSTM IP cores can be evaluated on logiCRAFT2 and logiCRAFT3 Xylon development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. Both platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. The platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: info@logicbricks.com
URL: www.logicbricks.com/html/evaluation_boards.htm

Ordering Information

This product is available directly from Xylon under the terms of the SignOnce IP License. Please contact Xylon for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Xylon or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

<table>
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<th>Version</th>
<th>Date</th>
<th>Note</th>
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<td>1.00</td>
<td>03.03.2009</td>
<td>New doc template</td>
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