Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc
Verification	Hardware validated
Reference Designs & Application Notes	Reference designs available for Xilinx ZC702/ZC706 development kits and the ZedBoard™ kit from Avnet Electronics Marketing
Additional Items	Bare-metal software driver Software drivers for different OS
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 SoC, Zynq UltraScale+™ MPSoC, UltraScale™/UltraScale+ and 7 series FPGA architectures, and other Xilinx All Programmable FPGAs
- Available software drivers for Linux and Microsoft® Windows® Embedded Compact OS
- Supports move operations, in positive and negative direction
- Supports 16 different ROP2 operations
- Porter-Duff composition with/without global alpha
- Integrated optional up/down bitmap scaling
- Integrated vertical and horizontal bitmap flipping
- Color-keyed transparency, source and destination
- Control of pixel alpha blending factors
- Anti-aliased 8-bit font expansion
- Pattern fill with 8x8 pixels patterns
- Solid fill with any of the supported color formats
- Supported color formats: RGB8, ARGB8, RGB16, ARGB16, RGB24 and ARGB24
- Configurable ARM® AMBA® AXI4-Lite bus compliant registers interface
- ARM® AMBA® AXI4 compliant master memory interface

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT[1)]	FF[1)]	IOB[2)]	BRAM Tile	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	mclk	rclk								
Kintex®-7 (XC7K325-2)	150	150	5929	4118	0	14	30	0	0	Vivado 2017.1
Zynq®-7000 (XC7Z045-2)	180	180	6369	4145	0	14	30	0	0	Vivado 2017.1
UltraScale+™ (XCZU9EG-1)	214	214	6226	4170	0	14	30	0	0	Vivado 2017.1

Notes:
1) Assuming the following configuration: 32-bit AXI4-Lite register interface with non-readable registers, 64-bit AXI4 memory interface (source and destination area) with 16-word burst size, implemented move and pattern fill with ROP2, transparency, solid fill, 8-bit anti-aliased font expansion and Porter-Duff composition with use of global alpha.
2) Assuming register and memory interfaces, as well status signals are connected internally.

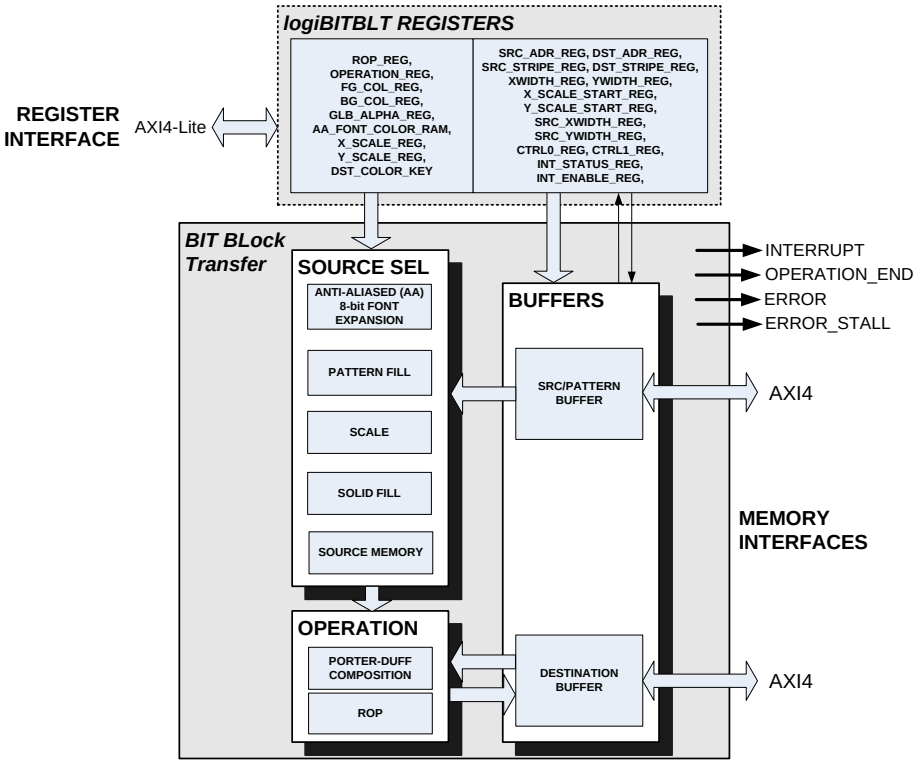

Figure 1: logiBITBLT Architecture

- Contiguous and array image addressing modes
- Supported configurable Big/Little Endianness memory layout

Features (cont)

- Internal FIFOs implemented as Block RAMs or distributed (LUT) RAMs
- Prepared for Xilinx Vivado® Design Suite (IP Integrator)
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Plug'n'play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiCVC-ML (Compact Video Controller with Multilayer Alpha Blending) and logi3D (Scalable 3D Graphics Accelerator)

Applications

- All kinds of GUI based embedded systems
- Car infotainment and telematics
- Industrial measurement equipment
- Medical devices
- Electronic gadgets, etc.

General Description

The logiBITBLT is a BIT Block Transfer 2D graphics acceleration IP core from Xylon logicBRICKS IP library, optimized for Xilinx All Programmable SoC and FPGAs and designed to accelerate rendering of computer graphics in GUI based embedded systems. The logiBITBLT IP core transfers blocks of graphics data (bitmaps) from one (source) to another (destination) memory region. These transfers are very fast and move the bitmaps from/to the on-screen or off-screen video memory. The IP can also move non-graphics data within system's memory and speed up general system tasks.

During data transfer the logiBITBLT IP core can perform various logical operations and create resulting bitmaps as combinations of source memory region content, a destination memory region content, and some pattern data. These operations can be combined with up and down scaling supported by an integrated optional bitmap scaler. In addition to raster operations, this IP can combine two bitmap images, and the global alpha blending factor, according to the Porter-Duff rules for composing images. The color-keyed transparency enables overlaying, while fonts' color expansion and anti-aliasing enable smooth fonts handling.

The logiBITBLT significantly increases performances of the most common graphic (GUI) operations, and at the same time frees the CPU for other system tasks. Even very cost-sensitive computing platforms can support attractive and responsive GUI interfaces by mean of the logiBITBLT IP core.

Xylon provides extensive software support for the logiBITBLT 2D graphics accelerator. As a part of standard IP core's deliverables, the bare-metal software driver simplifies IP use in FPGAs and assures the highest performance and determinism in Xilinx Zynq-7000 SoC designs that run with no operating system. Standard software drivers, which are available for Linux and Microsoft Windows Embedded Compact operating systems, enable software developers to work fast and efficiently with popular graphics libraries, widget toolkits and familiar development tools.

To learn more about available software support for Xylon graphics IP cores, please visit us online:
http://www.logicbricks.com/Products/Software-Drivers.aspx

The logiBITBLT IP core is fully embedded into Xilinx Vivado IP Integrator and ISE Xilinx Platform Studio implementation tools, and its integration with the on-chip AXI4 bus is very simple. Parametrizable VHDL design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiBITBLT can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores for building of advanced GUI embedded systems.

Functional Description

The logiBITBLT consists of the following blocks: Buffers, Source Selection, Operation and Registers. Figure 1 shows the internal IP core's structure.

Buffers

The bitmap data is stored in the source or destination buffers. These FIFOs optimize and increase the utilization of memory bandwidth. The Memory Address Generator sets the memory address prior to memory data read or write. The address is generated according to stripe length, color expansion, or reach of width/height bitmap values during the bit block transfer operation. The Memory Handshake Logic requests video memory access from the memory controller, supervises write operations to the Destination Buffer, and writes processed data back to the memory. The Destination Buffer optimizes and increases the utilization of memory bandwidth.

Source Selection

The bit block transfer Source Selection block controls the type of the source data. Following sources are available: solid color, source memory, pattern, anti-aliased 8-bit font expansion, and scale composition.
Anti-aliased 8-bit Font Expansion block is used for generating anti-aliased fonts.

Operation

The bit block transfer Operation block controls the type of the operation. Following commands are available: move, ROP and Porter-Duff composition. The Raster Operation block (ROP) performs logical operations between the source or pattern, and the destination bitmap. The Porter-Duff block executes composition rules for combining 2 bitmaps, with or without global alpha. The destination color key is used for color-keyed move operation.

Registers Module

The logiBITBLT's Registers module is a configurable module able to interface AXI4-Lite bus. A high registers' flexibility enables easier IP implementations in different SoC systems.

Registers module includes control, interrupt, operations, width and height, source and destination address and stripe, scaling setup, destination color key, global alpha, anti-aliased color RAM (CLUT) and IP version registers.

Core Modifications

The core is supplied in encrypted VHDL format compatible with Xilinx Vivado IP Integrator and ISE Xilinx Platform Studio implementation tools. Many logiBITBLT configuration parameters are selectable prior to VHDL core's code synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiBITBLT VHDL Configuration Parameters

Parameter	Description
C_USE_PAT_FILL	Implement pattern fill operation
C_USE_PORTER_DUFF	Implement Porter-Duff composition
C_USE_AA_FONT_EXPAND	Implement anti-aliased 8-bit font expansion operation
C_USE_GLOBAL_ALPHA	Use global alpha factor in Porter-Duff composition
C_USE_PD_DIV	Use post-divider in Porter-Duff composition
C_USE_SCALE	Implement scale operation
C_USE_SCALE_BILIN	Implement bilinear scaling or nearest neighbor
C_SCALE_LINE_SIZE	Size of line for scale operation
C_SCALE_STEP_INT	Number of integer bits for scaling factors and start scale values in corresponding registers
C_SCALE_STEP_FR	Number of fraction bits for scaling factors and start scale values in corresponding registers
C_USE_NEG_MOVE	Use move in negative direction
C_USE_BRAM	Internal buffers implementation type: Block RAMs or LUT RAMs
C_USE_SINGLE_COLOR_FORMAT	Implement support for a single color format
C_SELECT_COLOR_FORMAT	Select single color format
C_MEM_LITTLE_ENDIAN	Select between big or little endian memory layout
C_MEM_BYTE_SWAP	Select between swapped or non-swapped bytes on memory interface bus
C_MEM_DATA_WIDTH	Select memory data bus width: 32-bit, 64-bit or 128-bit
C_MEM_BURST_WIDTH	Select memory interface maximum burst size: 16, 32 or 64 words
C_READ_ALL_REGS	Select between readable or non-readable logiBITBLT registers. Non-readable registers reduce slice count and save FPGA resources
C_REG_BYTE_SWAP	Select between swapped or non-swapped bytes on register interface bus

There may be instances where source code modification is necessary. If you wish to adopt the logiBITBLT IP core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiBITBLT to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Memory Interface		
AXI4 source master interface	Bus	Refer to ARM's AMBA AXI4 specification
AXI4 destination master interface	Bus	Refer to ARM's AMBA AXI4 specification
Register Interface		
AXI4-Lite slave interface	Bus	Refer to ARM's AMBA AXI4 specification
Status signals		
interrupt	Output	Interrupt signal port, level sensitive, active high
operation_end	Output	Set when operation ends
error	Output	Set when memory address overflows
error_stall	Output	Set if logiBITBLT does not get access to memory in predefined period of time

Verification Methods

The logiBITBLT is fully supported by the Xilinx Vivado and ISE Design Suites. This tight integration tremendously shortens IP integration and verification. A full logiBITBLT implementation does not require any particular skills beyond general Xilinx tools knowledge. The ISE compatible version of the encrypted IP is shipped with compiled simulation libraries for Mentor Graphics' ModelSim. For information about Vivado compatible IP core simulations, please contact Xylon. The logiBITBLT evaluation IP core can be downloaded fron Xylon web site and fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logiBITBLT.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon provides free pre-verified reference designs to showcase the logiBITBLT graphics accelerator, other Xylon's logicBRICKS 2D and 3D graphics hardware accelerators and display controller IP cores on the most popular Xilinx Zynq-7000 AP SoC based development kits. Reference designs include evaluation logicBRICKS IP cores and hardware design files, OS image, software drivers, demo applications and documentation. To check a full list of Xylon reference designs please visit the web:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

logiREF-ZGPU Reference Design – evaluate 2D and 3D logicBRICKS graphics on Xilinx ZC702 Evaluation Board with connected PC monitor. Deliverables include complete software support for Linux OS, from the basic

FrameBuffer up to the full OpenGL® ES 1.1*. Configurable IP cores enable customization of the evaluation hardware, which can be also used with other popular operating systems.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000.aspx

logiREF-ZGPU-ZED Reference Design is functionally equal to the logiREF-ZGPU reference design – showcases the full 2D and 3D graphics engine running on the ZedBoard development kit from Avnet Electronics Marketing.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Zynq-AP-SoC-ZedBoard.aspx

logiREF-ZGPU-ZC706 Reference Design – evaluate 2D and 3D logicBRICKS graphics on Xilinx ZC706 Evaluation Board with connected PC monitor. Deliverables include complete support for Linux OS, from the basic FrameBuffer up to the full OpenGL® ES 1.1*. Configurable IP cores enable customization of the evaluation hardware, which can be also used with other popular operating systems.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000-ZC706.aspx

**Product is based on a published Khronos Specification, and is expected to pass the Khronos Conformance Testing Process. Current Conformance status can be found at www.khronos.org/conformance.*

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiBITBLT.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.04.	20.03.2009	Initial Xylon release – new doc template
1.05.	19.03.2010	Updated Table 1
1.05.	06.04.2010	New doc template
2.00.	15.12.2010	Document name changed
2.01.	04.01.2011	Document name changed
3.00.	13.12.2011	AXI4 memory interface added AXI4-Lite register interface added Interrupt signal port added, level sensitive, active high Document name changed
3.01.	05.03.2012.	Register layout fixed Document name changed
3.02.	24.04.2012.	Software reset option added Byte swapping on register interface and memory interface added Endianness correction on register interface and memory interface fixed
4.00.	15.06.2012.	Major changes in logiBITBLT: - removed PLB register and memory interface - removed XMB memory interface - separate AXI buses for source and destination memory access added - move in negative direction, color expansion and RLE decompression not supported - endianness correction for memory layout not supported - byte swapping on memory interface bus not supported
4.01.	13.09.2012.	Endianness correction added for memory layout (C_MEM_LITTLE_ENDIAN generic parameter) Byte swapping on memory interface bus added (C_MEM_BYTE_SWAP generic parameter) Support for 128-bit memory data bus width added
4.02.	14.10.2013.	Data sheet corrections Added new generic parameters: C_USE_ROP C_USE_SINGLE_COLOR_FORMAT C_SELECT_COLOR_FORMAT C_USE_SINGLE_PD C_SELECT_SINGLE_PD
5.00.	22.01.2014	Data sheet corrections. Removed generic parameters: C_USE_ROP C_USE_EXPAND C_USE_SINGLE_COLOR_FORMAT C_SELECT_COLOR_FORMAT C_USE_SINGLE_PD

Version	Date	Note
		C_SELECT_SINGLE_PD Features implemented by the above noted generic parameters are no longer supported. Added generic parameters: C_USE_SCALE C_SCALE_LINE_SIZE C_SCALE_STEP_INT C_SCALE_STEP_FR Restored move in negative direction operation
5.01.	18.03.2014	Data sheet corrections Restored generic parameters and corresponding features: C_USE_SINGLE_COLOR_FORMAT C_SELECT_COLOR_FORMAT Added generic parameters: C_USE_BRAM C_USE_NEG_MOVE
5.02.	16.06.2014	Document name changed according to the IP core
5.3.	02.03.2015	Document name changed according to the IP core Added generic parameters: C_USE_SCALE_BILIN Added information on logiBITBLT support in GPU Reference Design for Xilixn ZC706 Evaluation Board Document updated with information about Xilinx Vivado compatible logiBITBLT IP core
5.4.	08.09.2016	Document name changed according to the IP core Added generic parameter C_USE_PD_DIV Updated Table 1
5.5.	30.10.2017	Added support for Zynq UltraScale+ MPSoC and UltraScale/UltraScale+ FPGA architectures Updated Table 1