Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Features

- Supports Xilinx® Zynq®-7000 AP SoC, 7 Series and older Xilinx FPGA families
- Supports fast graphics operations with bitmaps
- 2.5D rendering – enables perspective corrected texture rendering in 3D
- Solid fill – rectangle rendering with any color
- Solid fill – triangle rendering with any color
- Triangle rendering with texturing: used for bitmap rotation, transformation or scaling
- Rectangle rendering with texturing: used for bitmap rotation, transformation or scaling
- Sub-pixel precision rendering
- Supports two different filtering methods:
  - bilinear interpolation
  - point sampling (the nearest neighbor interpolation)
- Texture swizzling storage option – for the highest speed texture rendering
- Clamp to edge texture rendering
- Supports 32bpp (True Color 24-bit with alpha channel) bitmap pixel memory layout
- Configurable registers interface compliant to ARM® AMBA® AXI4-Lite interface specifications

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraints (xdc)
Verification	Hardware validated
Reference Designs & Application Notes	
Additional Items	Bare-metal software driver

Simulation Tool Used
ModelTech's Modelsim

Support
Support provided by Xylon

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LCs	Slices[1] (FFs/ LUTs)	IOB	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	rclk									
Artix®-7 (XC7A35T-2)	125	190	11540	1803 (3144/6101)	0	0	2	13	0	N/A	Vivado 2014.4
Kintex®-7 (XC7K70T-3)	180	230	12307	1923 (3144/6201)	0	0	2	13	0	N/A	Vivado 2014.4
ZYNQ®-7000 (XC7Z010-2)	120	180	11117	1737 (3144/6101)	0	0	2	13	0	N/A	Vivado 2014.4

Notes:
1) Configuration with 32-bit AXI4 memory interface, AXI4-Lite register interface, texture cache depth of 4 kB, texture cache line size of 8 pixels. Source and destination bitmap coordinates width both set to 1024 pixels.

Features (cont):

- ARM AMBA AXI4 compliant configurable memory interface (32-bit or 64-bit)
- 7 Series FPGAs and Zynq-7000 AP SoC IP version prepared for Xilinx Vivado® Design Suite
- Spartan®-6, Virtex®-6 and older Xilinx FPGA families IP version prepared for Xilinx ISE® Design Suite
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Plug-and-Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiCVC-ML Compact Multilayer Video Controller, logiBITBLT Bit Block Transfer 2D Graphics Accelerator and logi3D Scalable 3D Graphics Accelerator

Applications

- All kinds of GUI based embedded systems
- Car infotainment
- Auto PCs, Hand-held PCs
- Personal Digital Assistants
- Set Top Boxes, Video Phones
- Electronic Gadgets, etc.

General Description

The logiBMP Bitmap 2.5D Graphics Accelerator is an IP core from Xylon logicBRICKS IP library, optimized for Xilinx All Programmable devices and designed to speed up graphics operations with bitmaps. The logiBMP Bitmap 2.5 Graphics Accelerator core significantly speeds up GUI rendering. It supports very complex bitmap operations like texture rendering, picture filtering, up and down scaling, and bitmap rotation. In combination with the logiBITBLT Bit Block Transfer 2D graphics accelerator it supports smooth transitions and animations, and adds a real "wow" effect to the GUI.

The logiBMP performs operations in one memory region (source block of data) and stores results to another memory region (destination block of data). It transforms and copies bitmaps from or to the video memory. Resulting (transformed) bitmap is created as a combination of the content of the source memory region and parameters stored in logiBMP registers.

The logiBMP IP core is fully embedded into Xilinx Vivado implementation tool, and its integration with the on-chip AXI4 bus is very simple. Parameterizable VHDL design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiBMP can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores for building of advanced GUI embedded systems.

Functional Description

The logiBMP graphics accelerator is partitioned into modules as shown in Figure 1: registers, bitmap buffer, triangle renderer, rectangle renderer, bilinear interpolation, and output buffer.
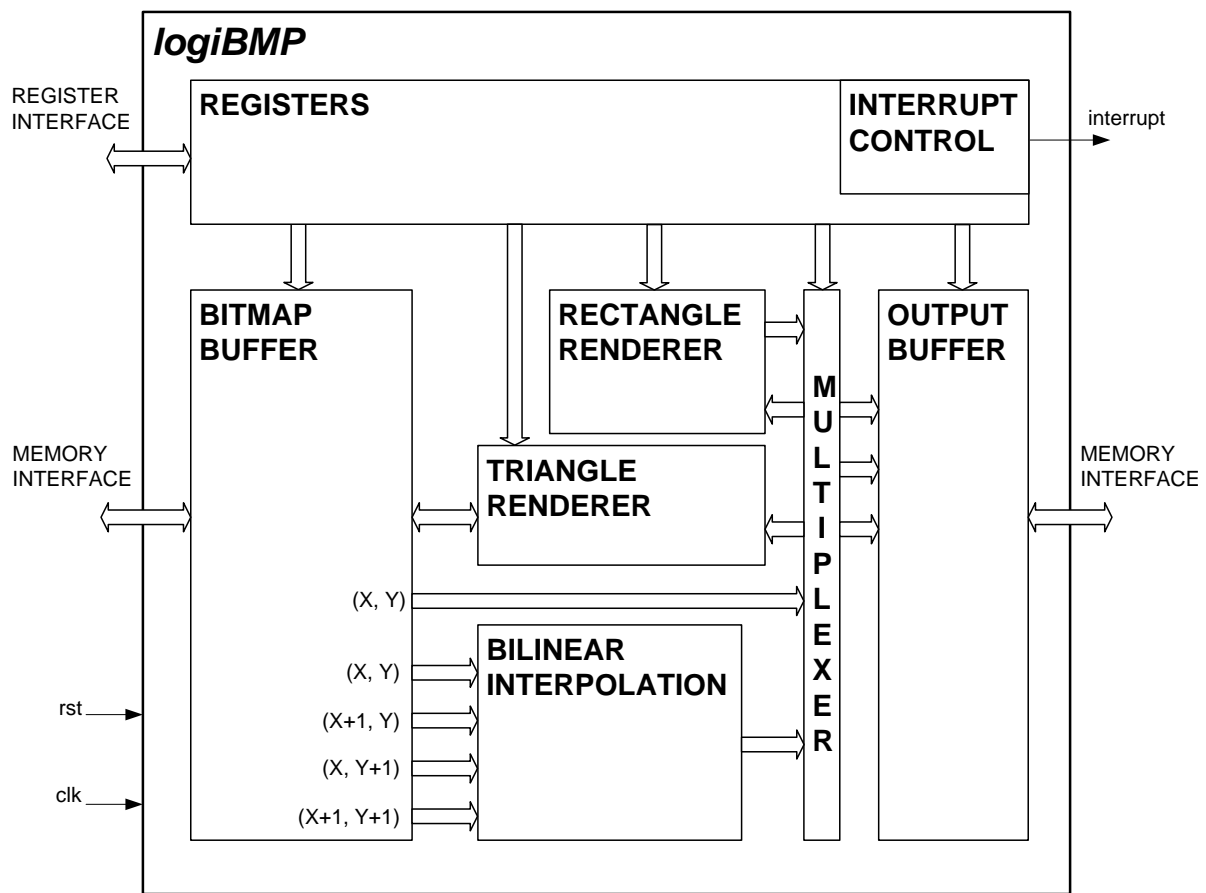
Figure 1: logiBMP Architecture

Registers

The register interface allows users to make real-time changes of the logiBMP parameters by software. The registers interface is configured as the AMBA AXI4-Lite compatible slave interface.

Bitmap buffer

Bitmap buffer fetches source bitmap (texture) from an external memory. Implemented bitmap cache increases the memory bandwidth utilization. Fast memory interface is configured as AMBA AXI4 compatible master memory interface.

Triangle renderer

The triangle renderer block renders triangle with a source bitmap. The triangle renderer calculates coordinates of pixels within the defined triangle, coordinates of corresponding texels (pixel in source bitmap – texture) for point sampling, and coordinates of neighboring texels for bilinear interpolation.

Rectangle renderer

The rectangle renderer block renders rectangle with a source bitmap. The rectangle renderer calculates coordinates of pixels within the defined rectangle, coordinates of corresponding texels (pixel in source bitmap – texture) for point sampling, and coordinates of neighboring texels for bilinear interpolation. Also solid fill - rectangle rendering operations are performed by the rectangle renderer. This block fills rectangles with the defined color, and its functions enable very useful graphics operations as, for an example, the clear screen function.

Bilinear interpolation

The bilinear interpolation block performs linear interpolation in both directions, first in the horizontal direction and then in the vertical direction. The block calculates resulting pixels from four neighboring pixels sourced by the bitmap buffer, and fraction parts of pixel coordinates sourced by the triangle renderer.

Output buffer

The output buffer stores processed pixels to the video memory. An implemented FIFO optimizes and increases the utilization of available memory bandwidth. The fast memory interface is configured as the AMBA AXI4 compatible master memory interface.

Core Modifications

The core is supplied in encrypted VHDL formats compatible with Xilinx Vivado IP Integrator and ISE Platform Studio implementation tools. Many logiBMP configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiBMP VHDL configuration parameters

Parameter	Description
C_READABLE_REGS	Readable registers: 0 – disable, 1 - enable
C_VIDEO_STRIDE_WIDTH	Video memory row stride: 9 – 512 pixels, 10 – 1024 pixels, 11 – 2048 pixels
C_USE_VIDEO_STRIDE_REG	Set OUTSTRIDE_REG register to define video memory row stride: 0 – disable, 1 – enable
C_XY_WIDTH	Maximal width of (x, y) coordinates
C_UV_WIDTH	Maximal width of (u, v) coordinates
C_CACHE_LINE_SIZE	Line size of texture cache: 4 – 4 pixels, 5 – 8 pixels, 6 – 16 pixels
C_CACHE_DEPTH	Depth of texture cache: 11 – 2kB, 12 – 4kB, 13 – 8kB, 14 – 16kB, 15 – 32kB

There may be instances where source code modification is necessary. If you wish to adopt the logiBMP IP core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiBMP to your requirements.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Memory Interface		
AXI4 Master Interface	Bus	Refer to ARM AMBA AXI4 specification
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to ARM AMBA AXI4 specification
Interrupt	Output	Interrupt output signal - active high, level sensitive

Verification Methods

The logiBMP is fully supported by the Xilinx Vivado and ISE Design Suites. This tight integration tremendously shortens IP integration and verification. A full logiBMP implementation does not require any particular skills beyond general Xilinx tools knowledge. The logiBMP evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logiBMP.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

If you wish to evaluate the logiBMP IP core in hardware, please contact Xylon and check for the reference design availability:

Email: info@logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.06	03.01.2011.	Initial Xylon release – new doc template
2.01	20.01.2012.	New features added: AXI4 memory interface; AXI4-Lite register interface; support for new Xilinx FPGA families (7 series). Updated logiBMP block diagram. Updated IP core's I/O signals.
2.02	09.10.2013.	Version updated according to IP core
2.2	12.03.2015.	Document updated with information about Xilinx Vivado compatible logiBMP IP core