Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	
Verification	Simulated and HW validated
Reference Designs & Application Notes	
Additional Items	Bare-metal SW driver
Simulation Tool Used	
Mentor Graphics' ModelSim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® 7 series FPGA, Zynq®-7000 All Programmable SoC and newer device families
- Compliant to ISO11898-1, CAN 2.0B and CAN 2.0A protocol specifications
- Supports both, standard (11-bit identifier) and extended (29-bit identifier) frames
- Supports bit rates up to 1 Mbps
- Receive message FIFO (up to 63 messages)
- Transmit message FIFO (up to 31 messages)
- Four programmable acceptance filters for message filtering
- Supports auto bit rate detection (bus listening mode) and internal loop-back mode
- Readable error counters and interrupt processing for all errors and message events
- ARM® AMBA® AXI4-Lite protocol compliant registers interface
- Low CPU overhead
- External CAN bus traansceiver required
- Fully synchronous, field proven design
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- IP deliverables include the software driver, documentation, and technical support
- Evaluation logiCAN IP core is available online

Table 1: Example Implementation Statistics[1] for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT	FF	IOB	RAMB36	RAMB18	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	aclk[2]	s_axi_clk									
Zynq®-7000 (XC7Z045-2)		100	944	1088	0	1	0	0	0	0	Vivado 2018.2
Artix®-7 (XC7A200-2)		100	873	1086	0	1	0	0	0	0	Vivado 2016.1
Zynq UltraScale+ (XCZU9EG-1)		100	864	1086	0	1	0	0	0	0	Vivado 2016.1

Notes:
1) Assuming: 31 TX buffers, 63 RX buffers, TQ prescale 4, enabled ID masking, 32-bit AXI4-Lite register interface.
2) Not used. The IP core requires an additional external clock signal (multiple of 8MHz) to support standard CAN timings.

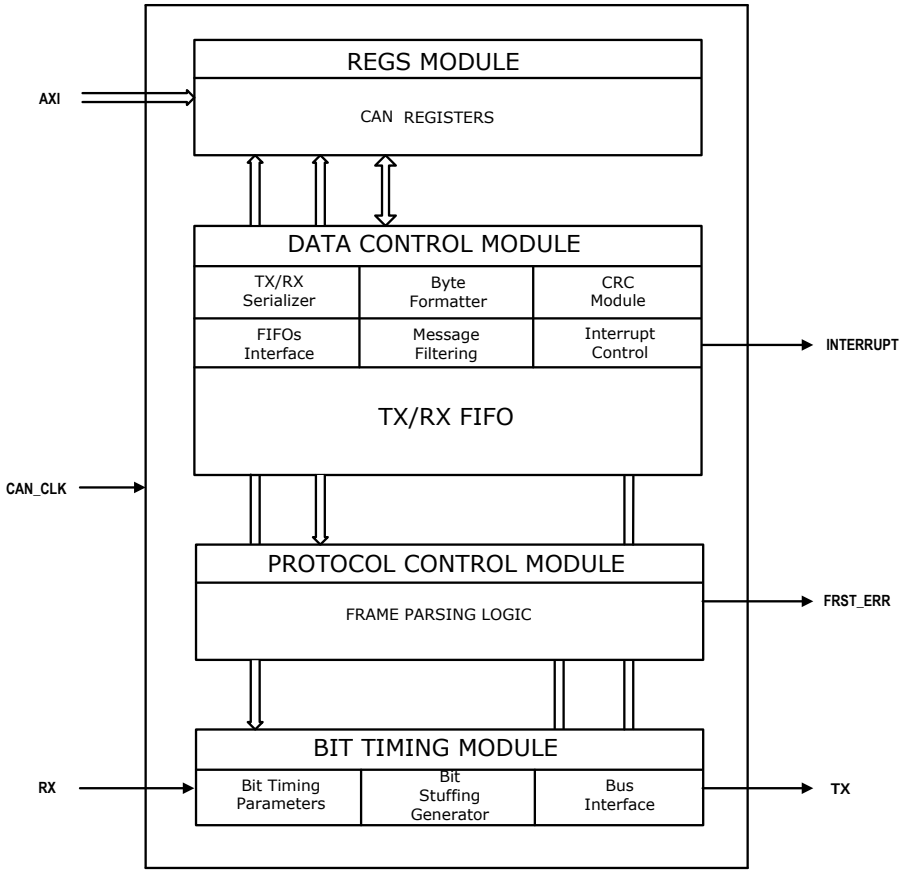

Figure 1: logiCAN Architecture

Applications

The logiCAN core can be used in a broad range of applications that use the CAN networking due to its speed, high security and efficiency. The range of applications includes the simple multiplex wiring systems as well as the highly integrated automotive, or building management applications.

Small logiCAN size enables implementation of multiple CAN controllers on a single FPGA or SoC device.

General Description

The logiCAN core supports ISO11898-1, CAN 2.0B and CAN 2.0A specified protocol functions. It provides all features expected from the standard CAN controllers including global masking (acceptance filtering) with 4 masks for the Standard or Extended CAN frames, fault confinement, stuff bit generation, CRC and arbitration handling. The ISO11898-1 TTC (time triggered communication) option is not supported.

What makes logiCAN different from other CAN controllers is its highly automated message handling. The CPU, released from the continuous CAN controller handling, can be used for other system tasks. It is extremely important for efficient low-cost systems.

Simple fill of the TX buffer (TX FIFO) starts a frame (message) transmission and all further actions, such as bus monitoring, arbitration loss, or the frame retransmission in the bus error case, are handled by the logiCAN with no CPU interventions. Multiple RX buffers (RX FIFO) ensure full frame reception, even at the highest baud rates. Only error-free, mask complying (pass-through acceptance filters) messages are stored, while others are checked, acknowledged and simply discarded. In mixed CAN networks, with standard and extended frames present on the same bus, an automatic frame type recording is assured.

Functional Description

The logiCAN core consists of: Regs module, Data Control module, Protocol Control module and Bit Timing module. The internal structure is shown in the block diagram - Figure 1.

Regs module

The Regs module features all logiCAN registers. IP core's operations are controlled and monitored by the Control and the Status registers. Set-up registers for message filtering, as well as error counters and bit timing registers, are also parts of the Regs module.

Data Control module

This module accepts the serial input from the CAN bus, parses it, and stores into internal buffers. Data from TX buffer is loaded into output shift register. RX and TX FIFOs are realized in a single Block RAM. The number of TX and RX buffers is configurable. CPU has 32-bit wide access to FIFO, while the CAN control logic has 8-bit wide access to this Block RAM. Each of 31 TX and 63 RX buffers uses 16 bytes of FIFO memory space. The RX/TX buffer (one FIFO location) is visible as four 32-bit storage locations to the CPU. TX buffer is visible at the beginning of FIFO memory space, while the RX buffer follows immediately. There must be at least one TX buffer and one RX buffer. Both, RX and TX buffers are independently handled in a circular buffer fashion. Acceptance filtering (global masking filters) for Standard and Extended frames are provided. The CRC sub-module generates and checks an appropriate CRC sequence. Interrupt processing for all errors and message exchange is done in Interrupt sub-module.

Protocol Control module

The Control module is the core of the logiCAN IP core. It implements the majority of control logic: bus states control, CAN frame parsing, error recognition, receive and transmit logic and complete fault confinement supporting logic.

Bit Timing module

CAN networks are built by a number of network nodes. Since network node is clocked with its own oscillator, the clock phase shift is present. The CAN protocol specifies a special synchronization algorithm to compensate phase shift. Bit timings are programmable (SYNC, SETUP and HOLD), and the sampling point is adjustable.

Core Modifications

VHDL constants, listed in the Table 2, enable an easy customization of the logiCAN architecture.

Table 2: logiCAN VHDL configuration parameters

Parameter	Description
C_ID_MASKING	0, 1 – Disable/Enable Acceptance Filtering (global masking filters)
C_NUM_RX_BUFS	1 – 63
C_NUM_TX_BUFS	1 – 31
C_TQ_PRESCALE	0 – 15

Although the logiCAN has been constructed compliant to the CAN network protocol specifications, there may be instances where the source code modification is necessary. Please contact Xylon for any required modifications.

Core I/O Signals

The core signal names are shown in Figure 1 and described in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to ARM's AMBA AXI4 protocol specification
interrupt	Output	High Level sensitive interrupt signal
logiCAN Interface		
can_clk	Input	Clock for the CAN state machine
rx	Input	Receive input from the CAN transceiver
tx	Output	Transmit output to the CAN transceiver
frst_err	Output	First CAN bus error signal (diagnostic)

Verification Methods

The logiCAN has been field tested/proved in different large-scale production projects. Functional verification is performed by using C language Bosch referent CAN model as a gold reference.

Get the logiCAN evaluation version and learn more about this IP core:

URL: http://www.logicbricks.com/Products/logiCAN.aspx

Recommended Design Experience

The user should have experience in the following areas:

- ISO11898-1, CAN 2.0B and CAN 2.0A protocol specification
- ModelSim
- Xilinx Vivado Design Suite

Available Support Products

To learn more about the Xylon logicBRICKS IP cores and development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

CAN in Automation (CiA)

It is a non-profit trade association of international users and manufacturers. CiA provides technical, product and marketing information regarding Controller Area Network applications. Can be contacted directly at:

CAN in Automation e.V.
E-mail: headquarters@can-cia.de
Phone:: +49-9131-69086-0
Fax: +49-9131-69086-79
URL: www.can-cia.com/

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
2.01	20.03.2006.	Initial Xylon release – new doc template.
3.00	20.06.2012.	New doc template. New features added.
3.01	31.03.2016.	Added PLBv4.6 register interface. Table 1 updated.
3.2	20.07.2016.	Updated for Vivado Design Suite. Removed support for FPGA families older than 7 series. Removed PLBv4.6 register interface. Table 1 updated.
	06.09.2018.	Updated implementation statistics table - Table 1