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Core Facts

Provided with Core	
Documentation	Data Sheet
Design File Formats	Encrypted VHDL
Constraints Files	XDC
Reference Designs & Application Notes	Reference Design for the ZC706 from Xilinx
Additional Items	SW support integrated with Linux and Microsoft® Windows® Embedded Compact drivers for graphics logicBRICKS IP cores
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim® Aldec Active-HDL™ and Riviera-PRO™	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® 7 Series, UltraScale™ and UltraScale+™ SoCs and FPGAs
- Provides twelve independent clock outputs that can be configured by generic parameters:
  - Six outputs can be dynamically configured through register interface during operation
  - Six outputs can be configured by generic parameters only
- Supports phase-locked loop (PLL) and mixed-mode clock manager (MMCM). The user can select clock primitive through IP configuration GUI
- Selectable output buffer type on clock output ports: BUFG, BUFH and no buffer
- Configurable through AXI4-Lite interface
- Software support for Linux and Microsoft® Windows® Embedded Compact operating systems
- Available for Xilinx Vivado® IP Integrator

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	LUT	FF	IOB[2]	PLL/MMCM	BRAM Tile	DSP48	BUFGCTRL	BUFHCE	Design Tools
Zynq®-7000[3] (XC7Z045-2)	384	853	0	2/0	0	0	3	0	Vivado® 2017.4
Zynq®UltraScale+™[4] (XCZU9EG-1)	402	854	0	2/0	0	0	3	0	Vivado® 2017.4

1) Assuming the following configuration: AXI4-Lite registers interface, Dynamic Reconfiguration Parameters Module (DRP) enabled, three clock outputs from logiCLK are used.
2) Assuming register interface, as well as status signals and generated clock outputs are connected internally.
3) The same implementation statistics apply to the Xilinx 7 series FPGAs.
4) The same implementation statistics apply to the Xilinx UltraScale and UltraScale+ FPGAs.

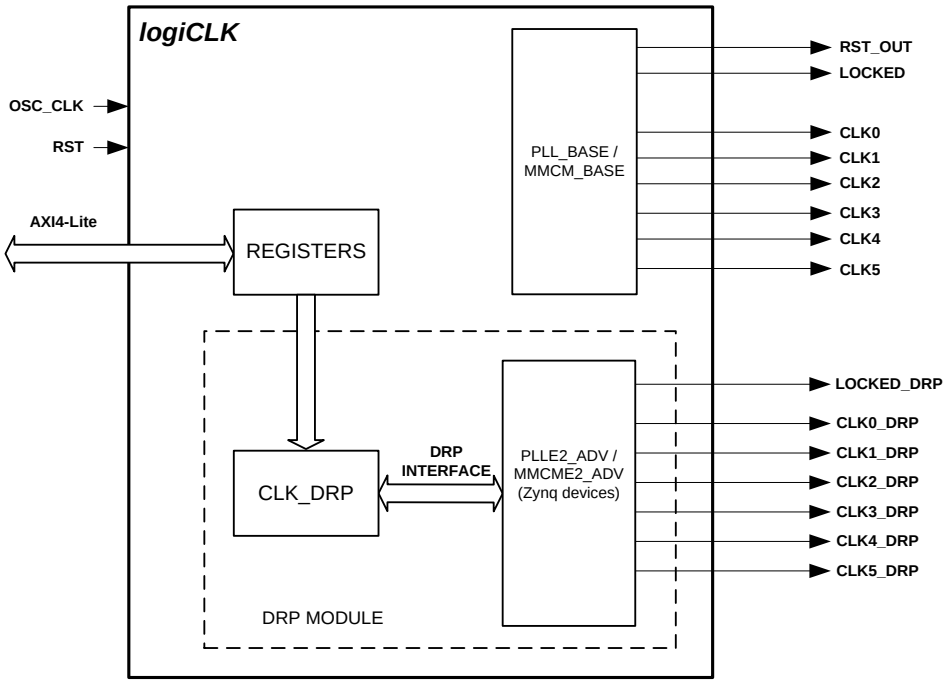

Figure 1: logiCLK Architecture

Features (cont.)

- Input clock frequency range*:
  - 7 series PLLs: 19 – 1066 MHz
  - 7 series MMCMs: 10 – 1066 MHz
  - UltraScale and UltraScale+ PLLs: 70 – 1066 MHz
  - UltraScale and UltraScale+ MMCMs: 10 – 1066 MHz
- Output clocks frequency range*:
  - 7 series PLLs: 6.25 – 741 MHz
  - 7 series MMCMs: 4.69 – 1066 MHz
  - UltraScale PLLs: 4.69 – 850 MHz
  - UltraScale MMCMs: 4.69 – 850 MHz
  - UltraScale+ PLLs: 5.86 – 891 MHz
  - UltraScale+ MMCMs: 6.25 – 891 MHz

** Depending on the sub-family and device's speed grade. Please consult the corresponding family data sheet.*

General Description

The logiCLK Programmable Clock Generator IP core from the Xylon logicBRICKS IP core library is optimized for Xilinx 7 Series, UltraScale and UltraScale+ SoC and FPGA devices, and designed to provide frequency synthesis, clock network de-skew and jitter reduction. Input and output frequency ranges are restricted by PLL, MMCM and Clock Buffer switching characteristics of the specific Xilinx All Programmable device.

The logiCLK clock generator IP core has twelve independent and fully configurable clock outputs. While six clock outputs can be fixed by generic parameters prior to the implementation, the other six clock outputs can be either fixed by generics or dynamically reconfigured in a working device. The Dynamic Reconfiguration Port

(DRP) interface gives system designers the ability to change the clock frequency and other clock parameters while the design is running by mean of a set of memory-mapped PLL/MMCM configuration and status registers (Figure 1).

The ability to dynamically change the clock signals during the operation is an important feature for some SoC applications. For example, the logiCLK IP core enables precise clock adjustments necessary for driving display output with different resolutions, which would be otherwise impossible without an external programmable Phase-Locked Loop (PLL)/Mixed-Mode Clock Manager (MMCM) device.

Xylon uses the logiCLK IP core in free and pre-verified Graphics Processing Unit (GPU) reference designs prepared for popular Xilinx Zynq-7000 AP SoC based development kits. Please visit Xylon web site to see the full list of logicBRICKS reference designs:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Xylon's software drivers for graphics logicBRICKS IP cores, such as the logiCVC-ML display controller IP core, include support for the logiCLK Programmable Clock Generator IP core and enable its easy use with the Linux and Microsoft Windows Embedded Compact operating systems.

Functional Description

The Figure 1 represents internal logiCLK architecture. The logiCLK functional blocks are Dynamic Reconfiguration Parameters module and Registers.

Dynamic Reconfiguration Parameters module

Dynamic Reconfiguration Parameters module is an optional IP core's module that provides six output clocks (CLK_DRP) defined by a set of re-configurable parameters. It is designed in accordance to the Xilinx Application Note XAPP888: "MMCM and PLL Dynamic Reconfiguration" for 7 Series, UltraScale and UltraScale+ FPGAs.

Registers

The CPU has access to logiCLK's registers through AXI4-Lite bus interface.

Core Modifications

The core is supplied in encrypted VHDL format compatible with Xilinx Vivado IP Integrator. Many logiCLK configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiCLK VHDL configuration parameters

Parameter	Description
C_OSC_CLK_FREQ_HZ	Oscillator frequency
C_RST_POLARITY	Reverts the polarity of input RST signal
C_CLK_PRIMITIVE_USE	Selects clock primitive PLL or MMCM.
C_USE_CLK_DRP[1)]	When set, enables the DRP module
C_USE_VLINK_CLK	When set, clkout0_drp is output from BUFIO for 7 series FPGAs.
C_CLKOUT0_BUFFER– C_CLKOUT5_BUFFER	Output buffer type on CLKOUT0-5 clock outputs. Available options are: No Buffer, BUFG and BUFH.
C_CLKOUT0_DRP_BUFFER– C_CLKOUT5_DRP_BUFFER	Output buffer type on CLKOUT0_DRP- CLKOUT5_DRP clock outputs. Available options are: No Buffer, BUFG and BUFH.
PLL Base Generics	
C_CLK_MULTIPLY[1)]	Specifies the multiplication value for all PLL CLK clock outputs
C_CLK0_DIVIDE – C_CLK5_DIVIDE[1)]	Specifies the divide value for PLL clock outputs 0 to 5
MMCM Base Generics	

Parameter	Description
C_MMCM_BASE_BANDWIDTH[1)]	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM
C_MMCM_BASE_DIVCLK_DIVIDE[1)]	Specifies the division ratio for all output clocks with respect to the input clock
C_MMCM_BASE_CLKFBOUT_MULT_F_R[1)]	Specifies the amount to multiply all CLKOUT clock outputs
C_MMCM_BASE_CLKFBOUT_PHASE_F[1)]	Specifies the phase offset in degrees of the clock feedback output.
C_MMCM_BASE_CLKOUT0_DIVIDE_F_R[1)]	Specifies the amount to divide the clock 0 output if a different frequency is desired
C_MMCM_BASE_CLKOUT1_DIVIDE[1)] – C_MMCM_BASE_CLKOUT5_DIVIDE	Specifies the amount to divide the associated clock output if a different frequency is desired
C_MMCM_BASE_CLKOUT0_DUTY_CYCLE_R[1)] – C_MMCM_BASE_CLKOUT5_DUTY_CYCLE_R	Specifies the duty cycle of the associated CLKOUT clock output in percentage
C_MMCM_BASE_CLKOUT0_PHASE_R[1)] C_MMCM_BASE_CLKOUT5_PHASE_R	Specifies the output phase relationship of the associated CLKOUT clock output in number of degrees offset
DRP PLL Generics	
C_DRP_CLKFBOUT_PHASE[1, 2)]	Specifies the phase offset in degrees of the clock feedback output
C_DRP_BANDWIDTH[1, 2)]	Specifies the PLL programming algorithm affecting the jitter, phase margin and other characteristics of the PLL
C_DRP_CLKFBOUT_MULT[1, 2)]	Specifies the multiplication value for all CLK_DRP clock outputs
C_DRP_DIVCLK_DIVIDE[1, 2)]	Specifies the divide ratio for all clock outputs with respect to the input clock
C_DRP_CLKOUT0_DIVIDE– C_DRP_CLKOUT5_DIVIDE[1, 2)]	Specifies the amount to divide the associated CLK_DRP clock output if a different frequency is desired
C_DRP_CLKOUT0_PHASE– C_DRP_CLKOUT5_PHASE[1, 2)]	Specifies the phase offset in degrees of the clock feedback output
C_DRP_CLKOUT0_DUTY– C_DRP_CLKOUT5_DUTY[1, 2)]	Specifies the Duty Cycle for CLK_DRP clock outputs in percentage
DRP MMCM Generics	
C_MMCM_DRP_BANDWIDTH[1, 2)]	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM
C_MMCM_DRP_COMPENSATION[1, 2)]	Clock input compensation, set to ZHOLD.
C_MMCM_DRP_DIVCLK_DIVIDE[1, 2)]	Specifies the division ratio for all output clocks with respect to the input clock
C_MMCM_DRP_CLKFBOUT_MULT_F_R[1, 2)]	Specifies the amount to multiply all CLKOUT clock outputs
C_MMCM_DRP_CLKFBOUT_PHASE_R[1, 2)]	Specifies the phase offset in degrees of the clock feedback output.
C_MMCM_DRP_CLKOUT0_DIVIDE_F_R[1, 2)]	Specifies the amount to divide the clock 0 output if a different frequency is desired
C_MMCM_DRP_CLKOUT1_DIVIDE[1, 2)] – C_MMCM_DRP_CLKOUT5_DIVIDE	Specifies the amount to divide the associated clock output if a different frequency is desired
C_MMCM_DRP_CLKOUT0_DUTY_CYCLE_R[1, 2)] – C_MMCM_DRP_CLKOUT5_DUTY_CYCLE_R	Specifies the duty cycle of the associated CLKOUT clock output in percentage
C_MMCM_DRP_CLKOUT0_PHASE_R[1, 2)] – C_MMCM_DRP_CLKOUT5_PHASE_R	Specifies the output phase relationship of the associated CLKOUT clock output in number of degrees offset

Notes:

1. Refer to Xilinx Clocking Resources User guides depending on the used device's family.
2. These parameters are used to configure CLK_DRP outputs if dynamic reconfiguration enable bit in control register is cleared, or if dynamic reconfiguration enable bit in control register set and data address is "0".

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
OSC_CLK	Input	Oscillator clock input
RST	Input	Global synchronous set/reset input
RST_OUT	Output	Synchronous set/reset output
LOCKED	Output	An output from the PLL/MMCM that indicates when the PLL/MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range
LOCKED_DRP	Output	An output from the PLL/MMCM that indicates when the PLL/MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range (if C_USE_CLK_DRP = 1)
Register Interface		
AXI4-Lite Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Clock Output Signals		
CLKOUT0_DRP-CLKOUT5_DRP	Output	User configurable (DRP) clock outputs (if C_USE_CLK_DRP = 1)
CLKOUT0-5	Output	User configurable clock outputs

Verification Methods

The logiCLK is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiCLK implementation does not require any particular skills beyond general Xilinx tools knowledge. This IP core has been successfully validated in different designs.

Software drivers

Xylon Linux Framebuffer driver includes the software support for the logiCLK IP core. For more information, please get the Linux Framebuffer User's Manual:

URL: http://www.logicbricks.com/Documentation/Datasheets/SW/Xylon-Linux-FrameBuffer.pdf

Xylon logiDISP driver for Microsoft Windows Embedded Compact includes the software support for the logiCLK IP core. For more information, please visit:

URL: http://www.logicbricks.com/Products/Xylon-Windows-Embedded-Display.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

logiREF-ZGPU-ZED Reference Design – evaluate 2D and 3D logicBRICKS graphics on the ZedBoard from Avnet Electronics Marketing with connected PC monitor. Deliverables include complete software support for Linux OS, from the basic Framebuffer up to the full 3D graphics. Configurable IP cores enable customization of the evaluation hardware, which can also be used with other popular operating systems. This design uses the logiCLK Programmable Clock Generator IP core to support different display resolutions.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Zynq-AP-SoC-ZedBoard.aspx

To check a full list of Xylon reference designs please visit the web:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00.	06.09.2012.	Initial Xylon release.
1.01.	28.03.2013.	Support for Spartan 6 FPGA families.
1.02.	20.09.2013.	Document version changed according to HW.
1.2.	08.12.2014.	New versioning scheme introduced for Vivado packaged IP core.
1.3	08.07.2016.	Removed support for Xilinx FPGA families older than 7 series. Removed PLB bus support.
1.3	03.11.2016.	Added LOCKED_DRP port to the block diagram on Figure 1 and to the Table 3.
1.4	21.02.2017.	Added support for MMCM in Xilinx 7 Series FPGA families. Updated example implementation statistics table, Table 1. Updated configuration parameters table, Table 2. Added buffer selection on clock output ports.
	20.12.2017.	Updated Table 1.
1.5	16.03.2018.	Added support for UltraScale and UltraScale+ families.