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Core Facts

Provided with the Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Verification/Validation	Simulated and HW validated
Reference Designs & Application Notes	logiREF-MULTICAM-ISP reference design for the Xylon logiISP-ZU-GMSL2 Evaluation Kit
Additional Items	logiISP-ZU-GMSL2 Evaluation Kit Stand-alone SW driver
Supported Simulation Tools	
Mentor Graphics ModelSim®, QuestaSim® and Aldec Active-HDL™	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Versal™ ACAPs, Zynq®-7000 SoCs, Zynq UltraScale+™ MPSoCs, UltraScale™, UltraScale+ and 7-Series FPGA devices
- Complete and configurable HDR pipeline includes:
  - Multiple Exposure Merge, supporting two or three exposures
  - Dynamic Range Compression
  - Brightness Enhancement
- Digitally processes and enhances the quality of the input video stream, optionally using multiple exposures to further enhance the quality of the output
- Supports video resolutions up to 7680x7680, including UHD 4K2Kp60 (3840x2160@60fps)
- Supports video input formats: RGB, color depth 8/10/12/14/16/20-bit per color
- Supports video output formats: RGB, color depth 8/10/12-bit per color
- Multiple channel video processing: 1, 2, 3 or 4 input video channels
- Parallel pixel processing with configurable number of pixels per clock: 1, 2 or 4
- Video input and output are ARM® AMBA® AXI4-Stream protocol compliant
- Optional registers are AMBA AXI4-Lite protocol compliant
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- Xylon offers MPSoC and ACAP reference designs and evaluation kits
- IP deliverables include the software driver, documentation, and technical support

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT	FF	IOB	RAMB36	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	aclk	s_axi_clk								
Zynq-7000 (XC7Z045-1)	150	150	3507	3875	0	11.5	66	0	0	Vivado 2020.2
Zynq UltraScale+ (XCZU9EG-1)	320	200	3506	3952	0	11.5	65	0	0	Vivado 2020.2
Versal ACAP (XCVC1902-2)	250	200	3723	3891	0	11.5	55	0	0	Vivado 2020.2

1) Assuming configuration: 1 12 bpc input channel and 8 bpc output, 1 pixel per clock processing, Dynamic Range Compression, Brightness Enhancement and AXI4-Lite interface.
2) Implementation statistics can vary depending on tool options, other FPGA design logic, speed grade, and other.

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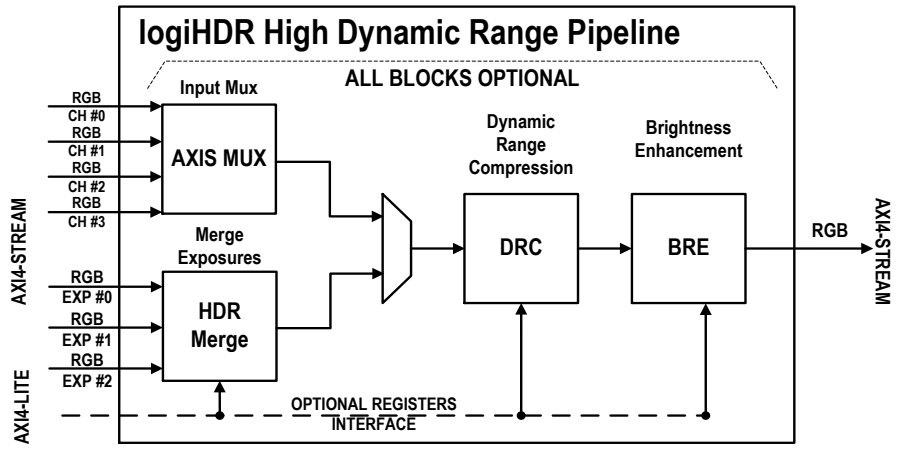

Figure 1: logiHDR Architecture

Applications

Application fields include Surveillance, Automotive Driver Assist, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

General Description

The logiHDR High Dynamic Range Pipeline IP core is an Ultra High Definition (UHD) HDR pipeline designed for digital video processing and image quality enhancements in embedded designs based on Xilinx FPGA, SoC, MPSoC and ACAP programmable devices. It enables processing of raw image data from HDR sensors and is able to extract maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by direct sunlight and objects placed in extreme shades.

Figure 2: Camera Video Input, Short Exposure

Figure 3: Camera Video Input, Long Exposure

Figure 4: HDR Processed Video Input from Camera

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The logiHDR IP core accepts RGB-formatted video inputs with different color depths and merges different exposures into a single HDR image; it dynamically enhances the luminance range, and enhances brightness in local areas. The logiHDR IP core can be combined with the logiISP-UHD Image Signal Processing (ISP) IP core in flexible and configurable video pipelines with advanced processing capabilities, such as removal of defective pixels, de-mosaicking of Bayer encoded video, image color and gamma corrections, advanced video noise filtering, video analytics used for control algorithms like Auto White Balance and Auto Exposure, and video data formats and color domains conversions.

The logiHDR IP core supports spatial resolutions up to 7680x7680, including the 4K2Kp60 (3840x2160@60fps) resolution, and accepts RGB video input format featuring different pixel color depths (8/10/12/14/16/20-bit per pixel). It outputs RGB-formatted processed video with pixel color depth independent from the input.

Figures 2, 3 and 4 illustrate video quality enhancements achievable by the logiHDR HDR pipeline IP core. Figure 4 shows the logiHDR video output after processing short and long exposure video input frames shown in Figure 2 and Figure 3.

The logiHDR IP core is AMBA AXI4 bus protocol compliant and can be smoothly integrated with other Xylon logicBRICKS, Xilinx, or third-party IP cores. In combination with other Xylon video and graphics logicBRICKS IP cores, the logiHDR can enhance the input image and output it to the display.

The logiHDR IP core's video input and video output interfaces conform to the AXI4-Stream video protocol and ensure low-latency video processing with no need for external video frame buffering. An optional AXI4-Lite-compliant registers interface ensures high flexibility and enables the processor to fully control the logiHDR HDR pipeline, changing its settings to adapt to the changes in the camera environment.

The logiHDR High Dynamic Range video pipeline IP core is prepackaged for the Xilinx Vivado IP Integrator (IPI) tool, it requires no skills beyond general tools knowledge, and can be used in same ways as Xilinx IP cores. Video system designers can easily set up the logiHDR HDR pipeline configuration by selecting video input and output formats, switching the pipeline stages (blocks) on and off, and setting up all parameters of the IP core through an easy-to-use IPI configuration GUI interface. I addition to the logiHDR IP core and software driver, Xylon also offers consultancy and design services; from HDR tuning for specific sensors (camera) to full turn-key video processing solutions.

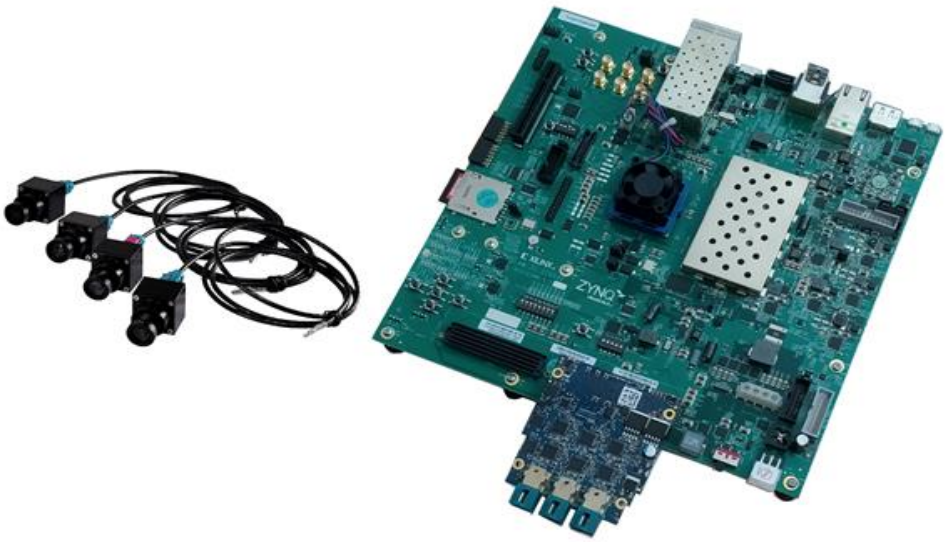

Figure 5: logiISP-ZU-GMSL2 HDR ISP Evaluation kit

To find out more about other evaluation options and learn more about upcoming video processing solutions, please contact Xylon at info@logicbricks.com.

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Functional Description

Figure 1 shows the logiHDR IP core's internal architecture. The logiHDR's functional blocks are as follows: HDR Merge, Dynamic Range Compression, Brightness Enhancement and logiHDR Registers.

HDR Merge (HDR)

The HDR Merge block performs real-time merging of two or three exposures of the same image. The precision of the HDR Merge block output (bits per color) is set through GUI, enabling trade-off between the resource consumption and the pixel processing precision.

Dynamic Range Compression (DRC)

The Dynamic Range Compression block is a perceptually-based global tone mapping operator which reduces the dynamic range of an HDR image acquired by the HDR Merge block, and preserves the details. It supports input bit depths of up to 20 bits per color, and outputs the image with bit depths of up to 12 bits per color.

Brightness Enhancement (BRE)

The Brightness Enhancement block performs a local brightness adjustment that carries out a per-pixel luminance correction, considering each pixel's local neighborhood in order to enhance the overall details visibility. It can also be used individually to enhance any SDR image that needs additional details improvement.

logiHDR Registers

The ARM AMBA AXI4-Lite-compatible logiHDR registers interface is optional and can be disabled prior to synthesis. The logiHDR IP configuration with no registers uses the hardwired HDR parameters setup through the IPI configuration GUI interface.

Multiple Channel Processing

Modern video systems often require data processing from multiple video inputs. Most of them are using the same processing algorithms. Processing each input separately increases the footprint on chip.

To achieve better FPGA utilization, the logiHDR supports shared logic for multiple channel data processing. When used in this configuration, the input AXI4-Stream multiplexer module can be instantiated at the input, or the incoming AXI4-Stream can already contain multiplexed channels.

The following logiHDR IP core blocks support multiple channel processing: Dynamic Range Compression and Brightness Enhancement.

Figure 6: Presentation of the Xylon logicBRICKS HDR ISP Evaluation kit

To see the multi-camera HDR ISP kit in action, please visit: https://www.logicbricks.com/Solutions/Xylon-HDR-ISP.aspx.

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Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator. Many logiHDR configuration parameters are selectable prior to the VHDL code synthesis, and the following table (Table 2) shows a selection from the list of available parameters:

Table 2: logiHDR VHDL Configuration Parameters

Parameter	Description
C_ACTIVE_ROWS	Default vertical resolution: 128 – 7680
C_ACTIVE_COLS	Default horizontal resolution: 256– 7680
C_MAX_COLS	Maximum horizontal resolution: 512, 1024, 2048, 4096, 8192
C_MAX_ROWS	Maximum vertical resolution: 512, 1024, 2048, 4096, 8192
C_S_AXIS_VIDEO_DATA_WIDTH	Input Color Data Width: 8, 10, 12, 14, 16, 20-bit
C_S_AXIS_VIDEO_MAX_SAMPLES_PER_CLOCK	Pixels per clock: 1, 2, 4
C_M_AXIS_VIDEO_DATA_WIDTH	Output Color Data Width: 8, 10, 12-bit
C_HAS_AXI4_LITE	Enable registers interface: 0, 1
C_HAS_DEBUG	Enable debug module: 0, 1
C_CORE_REGS_READABLE	Enable readability of core specific registers, configurable per block: 0, 1
C_USE_HDR	Enable HDR Merge block
C_NUM_OF_EXPO_HDR	Number of exposures on input: 2, 3
C_OUT_COLOR_WIDTH_HDR	Color data width on output from HDR: 10, 12, 14, 16, 18, 20
C_EXP_0_REG_HDR	Default Exp 0 Ratio
C_EXP_1_REG_HDR	Default Exp 1 Ratio
C_EXP_2_REG_HDR	Default Exp 2 Ratio
C_HIGH_VAL_REG_HDR	Default Highest Color Value
C_USE_DRC	Enable Dynamic Range Compression block
C_FILTER_TYPE_DRC	Type of DRC algorithm adaptation to lightning conditions
C_STRENGTH_DRC	Compression strength
C_STRENGTH_LMTR_DRC	Default strength limiter
C_PIXEL_THRES_DRC	Pixel Threshold for histogram statistics
C_GAIN_ADJ_DRC	Compression Gain Adjustment factor
C_DBL_BUF_DRC	Enable double buffer LUTs
C_USE_BRE	Enable Brightness Enhancement block
C_REFINE_BRE	Use Sample Refinement

The logiHDR is designed with regard to adaptability to various sensors (cameras). However, there may be instances where source code modification is necessary. Therefore, if you wish to adapt the logiHDR core to suit your specific needs and/or supplement the IP core's features set, you can allow us to tailor the logiHDR according to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins in order to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

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Table 3: Core I/O Signals

Signal	Signal Direction	Description
Streaming Video Interface		
AXI4-Stream Video Slave Interface #0	Bus	Refer to Xilinx AXI Reference Guide
AXI4-Stream Video Slave Interface #1	Bus	Refer to Xilinx AXI Reference Guide. Optional, present only if HDR Merge is enabled.
AXI4-Stream Video Slave Interface #2	Bus	Refer to Xilinx AXI Reference Guide. Optional, present only if HDR Merge is enabled and set to work with 3 exposures.
AXI4-Stream Video Master Interface	Bus	Refer to Xilinx AXI Reference Guide
Control Interface		
AXI4-Lite Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
Clock and Reset Signals		
aclk	Input	AXI4-Stream clock, shared between all streaming interfaces
aclken	Input	AXI4-Stream clock enable, shared between all streaming interfaces
aresetn	Input	AXI4-Stream reset, active low, shared between all streaming interfaces
s_axi_aclk	Input	AXI4-Lite clock
s_axi_aresetn	Input	AXI4-Lite reset, active low
Interrupt Interface		
irq	Output	Interrupt request, level sensitive, high active

Verification Methods

The logiHDR is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiHDR implementation does not require any particular skillset beyond general Xilinx tools knowledge.

Learn more about the logiHDR from:

URL: http://www.logicbricks.com/Products/logiHDR.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Camera systems

Available Support Products

The logiHDR IP core works with the logiISP-UHD Ultra High Definition (UHD) Image Signal Processing (ISP) pipeline IP core for digital processing and image quality enhancements of an input video stream in embedded video and vision designs based on Xilinx Zynq-7000 SoC, Zynq UltraScale+ MPSoC, Versal ACAP, 7 Series FPGA devices and newer devices.

The logiISP-UHD accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data, manipulated video data formats and color domains…:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiISP.aspx

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Xylon provides software Auto White Balance (AWB) and Auto Exposure (AE) libraries for use with the logiISP-UHD IP core. To get more information about these products, please contact Xylon:

Email: info@logicbricks.com

The logiISP-ZU-GMSL2 HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to develop multi-camera vision applications on Xilinx' Zynq UltraScale+ MPSoC devices. The complete hardware platform includes four of Xylon's 2.3MP automotive video cameras with the raw Bayer video output and supports the HDMI video output. Kit deliverables include the logiREF-MULTICAM-ISP reference design that demonstrates parallel HDR ISP processing of four video inputs.

URL: https://www.logicbricks.com/Solutions/Xylon-HDR-ISP-Pipeline.aspx

Ordering Information

This product is available directly from Xylon under the terms of Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	April 4th, 2016	Initial release
1.0	September 6th, 2018	Updated implementation statistics table – Table 1
1.1	October 16th, 2018	Document version changed to support new HW version. No changes to datasheet.
2.0	March 18th, 2021	Added multi-channel parallel video processing capabilities.
3.0	September 2nd, 2021	Improved BRE algorithm to prevent regional flickering. Improved timing constraints on BRE module. Fixed fetching incorrect image regions for bilinear interpolation of average values in BRE module. Updated implementation statistics table – Table 1 Added Figure 5 and Figure 6.
3.1	January 5th, 2024	A non-linear DRC algorithm option implemented for adaptation to daylight conditions.

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