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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Verification/Validation	Simulated and HW validated
Reference Designs & Application Notes	logiREF-VIDEO-HDR-ISP reference design for the Xylon logiUVK kit
Additional Items	logiUVK HDR UltraHD Video Kit Stand-alone SW driver
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim® Aldec Active-HDL™ and Riviera-PRO™	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, 7 Series and newer FPGAs
- Complete and configurable HDR pipeline includes:
  - Multiple Exposure Merge, supporting two or three exposures
  - Dynamic Range Compression
  - Brightness Enhancement
- Digitally processes and enhances the quality of the input video stream, optionally using multiple exposures to further enhance the quality of the output
- Supports video resolutions up to 7680x7680 including UHD 4K2Kp60 (3840x2160@60fps)
- Supports video input formats: RGB, color depth 8/10/12/14-bit per color
- Supports video output formats: RGB, color depth 8/10/12-bit per color
- Parallel pixel processing with configurable number of pixels per clock: 1, 2 or 4
- Video input and output are ARM® AMBA® AXI4-Stream protocol compliant
- Optional registers are AMBA AXI4-Lite protocol compliant
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- Can be evaluated on the logiUVK kit as a part of the 4K2K HDR UltraHD video pipeline reference design
- IP deliverables include the software driver, documentation, and technical support

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT	FF	IOB	RAMB36	RAMB18	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	aclk	s_axi_clk									
Artix®-7 (XC7A100T-1)[1]	125	150	3763	4389	0	4	3	51	0	0	Vivado 2015.4
Kintex®-7 (XC7K325T-2)[2]	175	200	3780	4389	0	4	3	51	0	0	Vivado 2015.4

1) Assuming minimum configuration: HDR Merge with 2 exposures, DRC, 8-bit output, 1 pix/clk, AXI4-Lite interface
2) BRE block can be used in the same configuration as above with additional 3250 LUT, 2230 FF, 6 BRAM, 24 DSP
3) Implementation statistics given for Artix-7 and Kintex-7 FPGAs are also valid for the Zynq-7000 AP SoC family
4) Implementation statistics can vary depending on tool options, other FPGA design logic, speed grade, and other

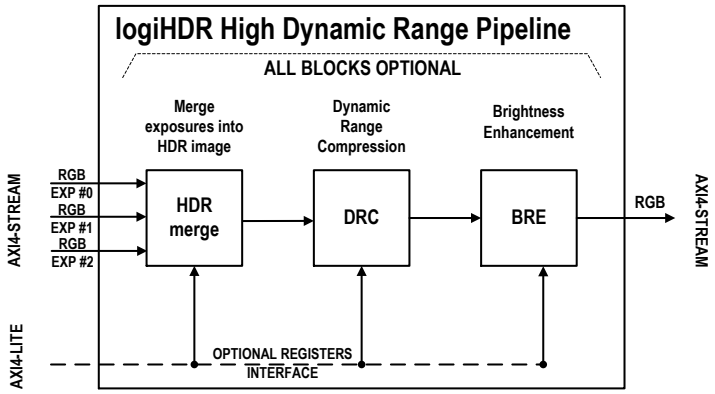

Figure 1: logiHDR Architecture

Applications

Application fields include Surveillance, Automotive Driver Assist, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

General Description

The logiHDR High Dynamic Range Pipeline IP core is an Ultra High Definition (UHD) HDR pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx Zynq-7000 All Programmable SoC, 7 Series FPGA devices and newer devices. It enables processing of the raw image data from HDR sensors and extracts the maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by a direct sunlight and objects placed in extreme shades.

The logiHDR IP core accepts RGB-formatted video inputs with different color depths and merges different exposures into a single HDR image, dynamically enhances the luminance range, and enhances brightness in local areas. The logiHDR IP core can be combined with the logiISP Image Signal Processing (ISP) IP core in flexible and configurable video pipelines with advanced processing capabilities, such as a removal of defective pixels, de-mosaicking of Bayer encoded video, image color and gamma corrections, advanced video noise filtering, video analytics used for control algorithms like Auto White Balance and Auto Exposure, and video data formats and color domains conversions..

The logiHDR IP core supports spatial resolutions up to 7680x7680 including the 4K2Kp60 (3840x2160@60fps) resolution and accepts RGB video input format featuring different pixel color depths (8/10/12/14-bit per pixel). It outputs RGB formatted processed video with pixel color depth independent from the input.

Figures 2, 3 and 4 illustrate video quality enhancements achievable by the logiHDR HDR pipeline IP core. The Figure 4 shows the logiHDR video output after processing of the short and long exposure video input frames shown on Figure 2 and Figure 3.

Figure 2: Camera video input, short exposure

Figure 3: Camera video input, long exposure

Figure 4 HDR processed video input from camera

The logiHDR IP core is AMBA AXI4 bus protocol compliant and can be smoothly integrated with other Xylon logicBRICKS, Xilinx, or third-party IP cores. In combination with other Xylon video and graphics logicBRICKS IP cores, the logiHDR can enhance input image and output it to the display.

The logiHDR IP core's video input and video output interfaces conform to the AXI4-Stream video protocol and assure low-latency video processing with no need for the external video frame buffering. An optional AXI4-Lite compliant registers interface assures high flexibility and enables processor to fully control the logiHDR HDR pipeline, changing its settings to adapt to the changes in the camera environment.

The logiHDR High Dynamic Range video pipeline IP core is prepackaged for Xilinx Vivado IP Integrator (IPI) tool, requires no skills beyond general tools knowledge, and can be used in same ways as Xilinx IP cores. Video system designers can easily setup the logiHDR HDR pipeline configuration by selecting video input and output formats, switching on and off pipeline stages (blocks), and setting up all IP core's parameters through an easy-to-use IPI GUI interface.

Besides the logiHDR IP core and software driver, Xylon offers consultancy and design services; from the HDR tuning for the specific sensor (camera) up to the full turn-key video processing solutions.

The logiHDR and other Xylon image signal processing IP cores can be fully evaluated on the Xilinx Zynq-7000 AP SoC based logiUVK HDR UltraHD Video Kit (Figure 5). The logiUVK kit provides a complete 8MP video processing hardware platform for the Xylon reference design with an integrated logiHDR IP core (4 pixel/clock).

Figure 5: logiUVK Kit in the Transportation Case (not included with the kit)

To learn more about this kit, please visit:

http://www.logicbricks.com/Products/logiUVK.aspx

To find more about other evaluation options and to learn more about the upcoming video processing solutions, please contact info@logicbricks.com.

Functional Description

The Figure 1 presents internal logiHDR architecture. The logiHDR functional blocks are: HDR Merge, Dynamic Range Compression, Brightness Enhancement and logiHDR Registers.

HDR Merge (HDR)

The HDR Merge block performs real-time merging of two or three exposures of the same image. The precision of the HDR Merge block output (bits per color) is set through GUI, enabling trade-off between the resource consumption and the pixel processing precision.

Dynamic Range Compression (DRC)

The Dynamic Range Compression block is a perceptually based global tone mapping operator, which reduces the dynamic range of the HDR image acquired by the HDR Merge block while preserving details. It supports input bit depths of up to 20bits per color and outputs the image of up to 12 bits per color.

Brightness Enhancement (BRE)

The Brightness Enhancement block performs local brightness adjustment that carries out per pixel luminance correction considering each pixel's local neighborhood in order to enhance the overall details visibility. It can be also used individually to enhance any LDR image that needs additional details improvement.

logiHDR Registers

The ARM AMBA AXI4-Lite compatible logiHDR registers interface is optional and can be disabled prior to synthesis. The logiHDR IP configuration with no registers uses the hardwired ISP parameters setup through the IPI GUI interface.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator. Many logiHDR configuration parameters are selectable prior to the VHDL code synthesis, and the following table presents a selection from the list of the available parameters:

Table 2: logiHDR VHDL Configuration Parameters

Parameter	Description
C_ACTIVE_ROWS	Default vertical resolution: 128 – 7680
C_ACTIVE_COLS	Default horizontal resolution: 256– 7680
C_MAX_COLS	Maximum horizontal resolution: 512, 1024, 2048, 4096, 8192
C_MAX_ROWS	Maximum vertical resolution: 512, 1024, 2048, 4096, 8192
C_S_AXIS_VIDEO_DATA_WIDTH	Input Color Data Width: 8, 10, 12, 14-bit
C_S_AXIS_VIDEO_MAX_SAMPLES_PER_CLOCK	Pixels per clock: 1, 2, 4
C_M_AXIS_VIDEO_DATA_WIDTH	Output Color Data Width: 8, 10, 12-bit
C_HAS_AXI4_LITE	Enable registers interface: 0, 1
C_HAS_DEBUG	Enable debug module: 0, 1
C_CORE_REGS_READABLE	Enable readability of core specific registers, configurable per block: 0, 1
C_USE_HDR	Enable HDR Merge block
C_NUM_OF_EXPO_HDR	Number of exposures on input: 2, 3
C_OUT_COLOR_WIDTH_HDR	Color data width on output from HDR: 10, 12, 14, 16, 18, 20
C_EXP_0_REG_HDR	Default Exp 0 Ratio
C_EXP_1_REG_HDR	Default Exp 1 Ratio
C_EXP_2_REG_HDR	Default Exp 2 Ratio
C_HIGH_VAL_REG_HDR	Default Highest Color Value
C_USE_DRC	Enable Dynamic Range Compression block
C_STRENGTH_LMTR_DRC	Default strength limiter
C_DBL_BUF_DRC	Enable double buffer LUTs
C_USE_BRE	Enable Brightness Enhancement block
C_REFINE_BRE	Use Sample Refinement

The logiHDR is designed with regard to adaptability to various sensors (cameras). However, there may be instances where source code modification is necessary. Therefore, if you wish to adopt the logiHDR core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiHDR to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Streaming Video Interface		
AXI4-Stream Video Slave Interface #0	Bus	Refer to Xilinx AXI Reference Guide
AXI4-Stream Video Slave Interface #1	Bus	Refer to Xilinx AXI Reference Guide. Optional, present only if HDR Merge is enabled.
AXI4-Stream Video Slave Interface #2	Bus	Refer to Xilinx AXI Reference Guide. Optional, present only if HDR Merge is enabled and set to work with 3 exposures.
AXI4-Stream Video Master Interface	Bus	Refer to Xilinx AXI Reference Guide
Control Interface		
AXI4-Lite Slave Interface	Bus	Refer to Xilinx AXI Reference Guide

Signal	Signal Direction	Description
Clock and Reset Signals		
aclk	Input	AXI4-Stream clock, shared between all streaming interfaces
aclken	Input	AXI4-Stream clock enable, shared between all streaming interfaces
aresetn	Input	AXI4-Stream reset, active low, shared between all streaming interfaces
s_axi_aclk	Input	AXI4-Lite clock
s_axi_aresetn	Input	AXI4-Lite reset, active low
Interrupt Interface		
irq	Output	Interrupt request, level sensitive, high active

Verification Methods

The logiHDR is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiHDR implementation does not require any particular skills beyond general Xilinx tools knowledge.

Learn more about the logiHDR from:

URL: http://www.logicbricks.com/Products/logiHDR.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Camera systems

Available Support Products

Xylon provides the logiREF-VIDEO-HDR-ISP pre-verified reference design to showcase the logiHDR IP core and Xylon ISP pipelines on the Xilinx Zynq-7000 AP SoC based logiUVK HDR UltraHD Video Kit. The reference design contains everything you need to immediately start evaluating and working with the Xylon logiHDR: the SoC design including evaluation logicBRICKS IP cores, hardware design files, documentation and the GUI-based demo application (Linux OS):

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/HDR-ISP-Pipeline-for-Xilinx-All-Programmable.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	April 4th, 2016	Initial release