Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Reference Designs & Application Notes	Xilinx Vivado® IP Integrator reference design
Additional Items	– Reference design for Xilinx Zedboard – User space Linux drivers and demo software
Simulation Tool Used	
Mentor Graphics' ModelSim, Xilinx Vivado Simulator	
Support	
Support provided by Xylon	

Features

- Advanced HOG/SVM object classification core for camera-based video systems
- Enables object detection in camera systems
- Supports Xilinx® Zynq™-7000 SoC, Zynq™-UltraScale+™ MPSoC and Xilinx FPGAs
- Up to 4 SVM engines for multiple objects searching in parallel (compile time configurable)
- Object models loadable run-time via software
- Maximum input image size: 2048x2048 (customizable up to 4096x4096)
- Integrated scaler for multi scale detection (image pyramid)
- Search area definition (even partially out of the image)
- ARM® AMBA® AXI3/AXI4 Master Interface (input/output data transfer from/to DDR)
- ARM® AMBA® AXI4 Lite Memory Mapped Register Interface
- High bandwidth (>600 Mpixels/sec)
- High throughput (>9.3M classifications/sec, >38.4 GMAC/sec)
- Low Latency (< 8 lines)
- Fully programmable (instruction based control flow)
- A pedestrian detection classifier trained on a wide range of automotive scenarios is available
- Software tool available for simple training of new object models
- Xilinx Vivado® ref. design and demo software

Applications

- Driving Assistance Systems
- Machine learning
- Video Surveillance
- Robot Navigation

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) [1] sysgen_clk	LUTs[2]	FFs[2]	IOB	CMT	BRAM[3]	DSP48A	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z020-1)	200	4,105	5,533	0	0	23	33	0	N/A	VIVADO® 2017.4
Zynq®-UltraScale+ (XCZU9EG-2)	300	3,962	5,584	0	0	23	33	0	N/A	VIVADO® 2017.4

Notes:

1) The maximum pixel rate is half Fmax
2) Assuming configuration with default IP parameters, max image size = 2048x2048, max template size = 128x64, 1 SVM. Each additional SVM requires 696 FFs, 562 LUTs, 3,5 BRAMs and 31 DSP48s.
3) Number of RAMB36

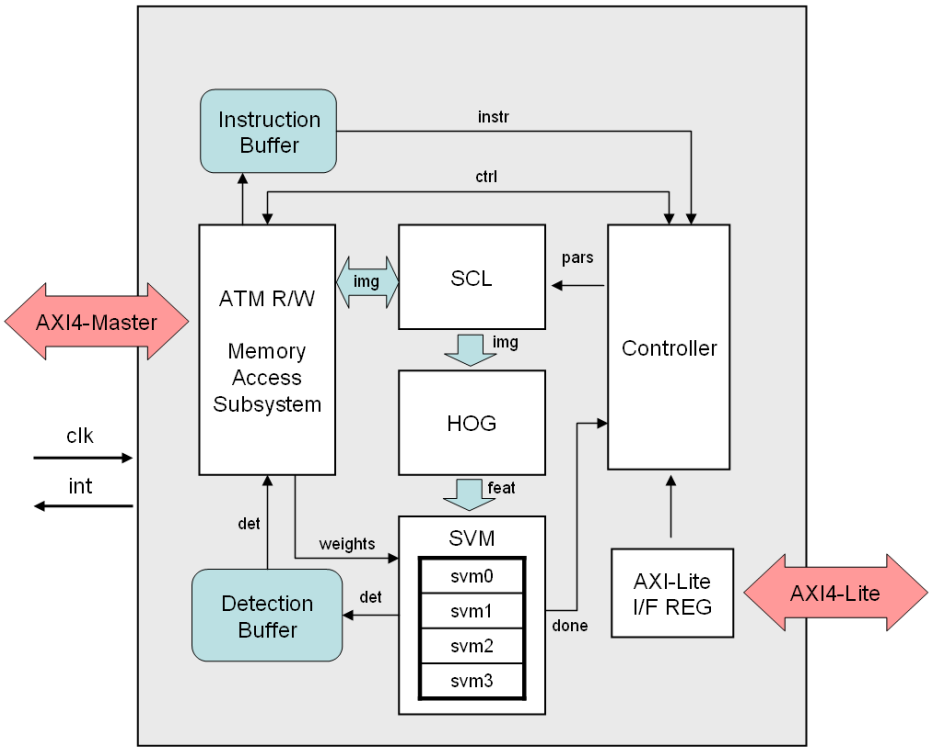

Figure 1 : logiHOG Architecture

General Description

logiHOG is a learning-based object detection IP core from the Xylon logicBRICKS library, which is developed for embedded vision systems. The logiHOG implements an advanced classification algorithm that follows a discriminative approach. It combines a HOG-based descriptor and a SVM classifier.

The HOG (Histogram of Oriented Gradients) is a descriptor designed to encode the structure of objects. The SVM (Support Vector Machine) is a non probabilistic binary linear classifier.

The logiHOG IP core streams out the input frames from the external memory, internally generates a pyramid of images at different scales, and finally classifies a detection window sliding over the entire pyramid in order to detect differently sized objects, or the objects moving in an arbitrary range. Depending on the trained model, the logHOG may detect different objects, such as pedestrians, vehicles, traffic signs, faces, etc. Users may load their own classifiers via the provided software API at the run-time. At the compile time, multiple SVM engines can be instantiated to increase the throughput and to enable parallel detections of different objects..

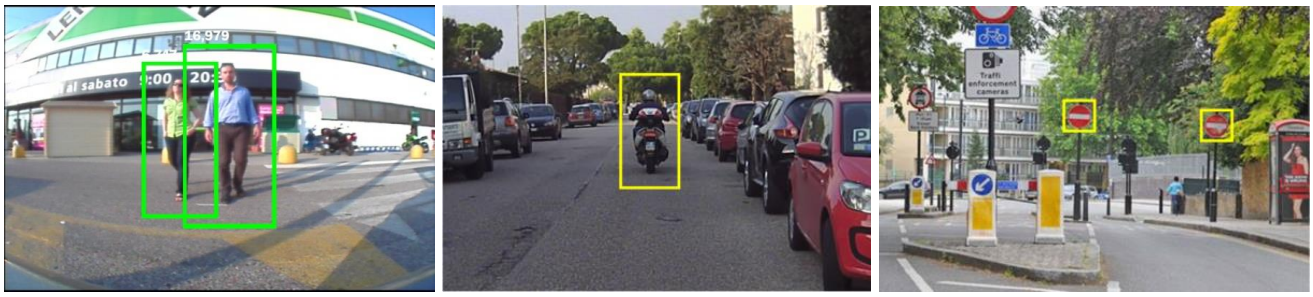

Figure 2: Examples of detectable objects

Functional Description

The Figure 1 presents internal logiHOG IP core's architecture. The logiHOG functional blocks are: Controller, Instruction Buffer, Memory access subsystem, AXI-Lite I/F REG, SCL, HOG, SVM and Detection Buffer.

Controller

logiHOG (since version 3.0) is a core programmable through a specific instruction set. The Controller module rules the logiHOG execution flow. It fetches instructions from the Instruction Buffer, decodes them, and configures and controls the other subsystems accordingly.

Instruction Buffer

The Instruction Buffer contains the list of instructions that must be executed by the Controller.

Memory access subsystem

The memory access subsystem is responsible for read/write data transfer operations from/to the external memory through the AXI4 master interface.

AXI-Lite I/F REG

A bank of internal R/W registers is available to control logiHOG via software through the AXI4-Lite interface.

SCL

The SCL module is responsible for generating the pyramid of images at different resolutions to be processed by the HOG module. The scaling process is performed using bilinear interpolation with anti-aliasing to avoid typical artifacts in downscaling images.

HOG

The HOG module receives scaled regions of interest from SCL and extracts a dense map of the HOG features. The computation is done online without any buffering to external memory: a HOG feature vector is computed for each valid position of the detection window in the image.

SVM

The SVM module is responsible for classifying features computed by the HOG module. It returns the set of positions which are classified as positives (i.e. object). The results of the detection are stored in the Detection Buffer. Classifiers can be described as a vector of coefficients (weights and a bias value) generated during the training process. Classifiers are loaded at run-time into the core via the AXI4 Master Interface. Up to four SVM modules can be instantiated into the core and work in parallel to detect different objects simultaneously on the same input image. The computation is strongly parallelized to increase the global throughput.

Detection Buffer

Results of the detection process are stored in the Detection Buffer before being moved to external memory via the AXI4 Master Interface. Each result consists of a descriptor for the detection (positive) found in the input image. The descriptor holds information such as the ROI index (thus the scale at which it was detected), its x-y position, the classifier index that performed the detection and a score qualifier.

Core I/O Signals

Descriptions of all signals I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk	Input	Input processing clock
reset	Input	Global reset input, high active
Memory Interface		
AXI4 Interface	BUS	Refer to AMBA AXI version 4 specification from ARM. Note: both Read and Write channels are used
Register Interface		
AXI4-Lite Interface	BUS	Refer to AMBA AXI version 4 specification from ARM
Auxiliary Signals		
interrupt	Output	Interrupt signal, level sensitive, high active

Verification Methods

The logiHOG IP core is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiHOG implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools

Available Support Products

The logiHOG IP core can be evaluated on the logiADAK Advanced Driver Assistance (ADAS) Development Kits that allow customers to fully evaluate performance on their vehicle or in the laboratory.

Xylon provides a software tool, named the logiSTK (Software Training Kit), for training and testing object detectors based on HOG/SVM classifiers. It is designed to support users in all the training process stages, in a simple and effective way.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0.1	29.06.2015	Initial datasheet release
3.0.1	02.05.2018	Core refectoring

The logiHOG core is sourced from Technology Partner
eVS embedded Vision Systems Srl.