logiHSSL High Speed Serial Link (HSSL) Slave Controller

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Reference Designs & Application Notes	Reference design prepared for the logiHSSL-ZU starter kit
Additional Items	logiHSSL-ZU HSSL Starter Kit
Supported Simulation Tools	
Mentor Graphics ModelSim®, QuestaSim® and Aldec Active-HDL™	
Support	
Support provided by Xylon	

Features

- Enables easy interfacing between Infineon AURIX™ TC2xx, TC3xx and TC4xx microcontrollers and AMD FPGA and SoC devices
- Slave controller IP core compatible with the High Speed Serial Link (HSSL) native interface from Infineon Technologies AG
- Aimed at safety-critical automotive applications
- Low pin count (2 x 2 LVDS, 1 x clock)
- Supports baud rates of up to 320 Mbaud/s at a net payload data-rate of up to 84%
- HSSL Sleep function is not supported
- 4 HSSL channels, initiator and target, (full configuration); 1 target and one Stream channel (reduced)
- Optional debug ports for debugging during system integration
- Implements ARM® AMBA® AXI4–Lite Slave bus compliant interface and enables easy access to internal registers inside the logiHSSL IP
- Implements ARM AMBA AXI4 Master bus compliant interface that enables logiHSSL IP an easy access to 3 GB of local AMD device addressable space (from 0x00000000 to 0xBFFFFFFF). This enables AURIX microcontroller to access:
  - Registers and on-chip RAM in programmable logic (access to internal register spaces of other IPs)
  - Register space and On-Chip Memory (OCM) in the processing system through High priority ports.
  - On-board linearly addressable Flash memory
  - On-board DDR memory through local memory controllers
- logiHSSL-ZU FPGA HSSL Starter Kit is available from Xylon
- Supports AMD Zynq™ 7000 and Zynq™ UltraScale+™ SoCs, Series 7, UltraScale™ and UltraScale+™ FPGAs
- Prepared for the AMD Vivado™ Design Suite

Table 1: Example Implementation Statistics for AMD Adaptive SoCs

Family (Device)	Fmax (MHz)	LUT	FF	IOB	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
Artix 7 (xa7a15t-cpg236-1Q)	80	5161[1)]	4582[1)]	4	0	0	0	0	0	Vivado™ 2021.2
Zynq™ UltraScale+™ (xczu9eg-ffvb1156-2)	80	5086[1)]	4624[1)]	4	0	0	0	0	0	Vivado™ 2021.2
Zynq™ UltraScale+™ (xczu9eg-ffvb1156-2)	80	2631[2)]	2399[2)]	4	0	0	0	0	0	Vivado™ 2021.2

1. Assuming configuration: No debug ports.

2. Assuming configuration: No debug ports, reduced functionality.

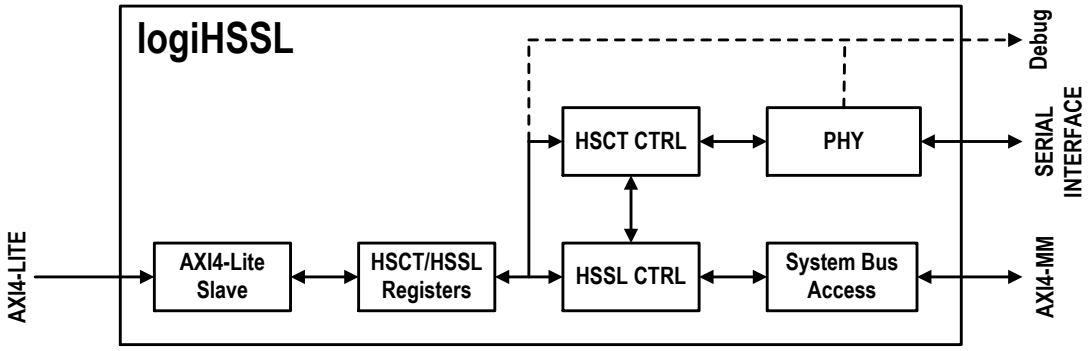

Figure 1: logiHSSL Architecture

Applications

Emerging automotive and industrial applications, such as the Advanced Driver Assistance (ADAS) and Automated Driving (AD), are both performance hungry and safety-critical. Typically the supporting system architectures use AMD FPGA and SoC devices for data aggregation, pre-processing and data distribution tasks, and the Infineon AURIX microcontrollers to provide the ASIL D level functional safety.

General Description

The logiHSSL IP core enables high-speed communication between microcontrollers of Infineon's AURIX family (TC2xx and TC3xx) and adaptive AMD SoC (System-on-Chip) and FPGA (Field Programmable Gate Arrays) devices via the Infineon High Speed Serial Link (HSSL). This serial link supports baudrates of up to 320 Mbaud at a net payload data-rate of up to 84%.

The new IP core allows system designers to combine functional safety and security provided by AURIX with the wide range of functional possibilities brought to the table by AMD devices. Linked devices can access and control each other’s internal and connected resources through the HSSL link.

Starting from version 2.0, the logiHSSL can be configured in a reduced mode that provides the main communication features. Compared to the full IP configuration, this reduced mode enables approximately 50% savings in programmable logic.

The logiHSSL IP is prepared for the AMD Vivado™ Design Suite to enable quick and efficient implementation in the latest AMD programmable devices, for use in the embedded systems that meet the highest safety standards.

Functional Description

The logiHSSL IP core is an IP block for the AMD Vivado™ development flow. It includes the embedded Infineon High Speed Serial Interface (HSSL) and a control unit to connect an external Infineon AURIX automotive microcontroller with AMD FPGA and/or ARM processing unit (SoC, MPSoC) for the purpose of the data exchange.

Four major modules can be identified in the architectural block diagram shown in Figure 1.

HSCT Layer

The HSCT layer is the implementation of the HSCT link layer. It is the physical layer of the HSSL protocol.

HSSL Control Unit

The HSSL control unit is the IP core's main module that facilitates the control over the HSSL protocol, which includes the HSSL layer (upper layer) and HSCT layer (lower layer). The control is interfaced to the CPU by means of a register set. There are separate register sets for HSSL and HSCT layer control.

AXI4–Lite Interface (Slave)

AXI4–Lite slave interface is used to access all IP core's registers within the HSSL control unit. It facilitates a bridge from the AXI4–Lite bus to the internal interconnect.

AXI4 Interface (Master)

IP core can access any AXI-addressable space in the FPGA/SoC through the AXI4 master interface. It facilitates a bridge from the internal logic to the AXI4 bus architecture, including the corresponding address remapping.

For more information on internal architecture of the HSSL protocol control (HSCT layer and HSSL control unit), see AURIX TC27x C-Step 32-Bit Single-Chip Microcontroller documentation from Infineon.

Core I/O Signals

Table 2: Core I/O Signals

Signal	Signal Direction	Description
AXI4 - Master Interface	Bus	Refer to ARM AMBA AXI4 specification*
AXI4 - Lite Interface	Bus	Refer to ARM AMBA AXI4 specification*
clk_400	Input	400 MHz clock used for sampling of the HSSL RX lines*
rst_400	Input	400 MHz reset
clk_200	Input	200 MHz clock used for sampling of the HSSL RX lines*
rst_200	Input	200 MHz reset
clk_160	Input	160 MHz clock used for data output on the HSSLTX lines*
hsct_irq_o	Output	HSCT interrupt signal
hssl_irq_o	Output	HSSL interrupt signal
lvdsrx_data_p	Input	LVDS HSSL serial input, positive
lvdsrx_data_n	Input	LVDS HSSL serial input, negative
lvdstx_data_p	Output	LVDS HSSL serial output, positive
lvdstx_data_n	Output	LVDS HSSL serial output, negative
dbg_slv_txen	Output	Debug output – internal TX enable (80 MHz).
dbg_lvdstx_smpl	Output	Debug output – internal TX data bus (80 MHz).
dbg_slv_clktsten	Output	Debug output – internal TX clock test enable (80 MHz).
dbg_slv_loopen	Output	Debug output – internal loop RX->TX enable (80 MHz).
dbg_lvdsrx_smpl	Output	Debug output – internal RX sample data bus (1600 Mbps, 80 MHz clock).
dbg_rx_low_speed	Output	Debug output – internal RX low speed active (80 MHz).
dbg_rx_high_speed	Output	Debug output – internal RX high speed active (80 MHz).
dbg_rx_ph_val	Output	Debug output – internal RX phase valid detected (80 MHz).
dbg_rx_ph_act	Output	Debug output – internal RX phase active (80 MHz).
dbg_rx_data	Output	Debug output – internal RX data byte (input to data stream processing) (80 MHz).
dbg_rx_data_val	Output	Debug output – internal RX data byte valid strobe (input to data stream processing, asserted for 1 clock on each byte received) (80 MHz).

* AXI4 Master and AXI4-lite Slave interfaces must work on 80 MHz clock, generated from the same clock source as the 160 MHz clock used for HSSL TX, as well as 400 MHz and 200 MHz clocks used for HSSL RX. It is preferred to use the clock reference from the HSSL Master.

Verification Methods

The logiHSSL is fully supported by the AMD Vivado™ (IPI) Design Suits. This tight integration tremendously shortens IP integration and verification. A full logiHSSL implementation does not require any particular skills beyond general AMD tools knowledge. For more information, please contact Xylon Technical Support:

Email: support@logicbricks.com

Recommended Design Experience

The user should have experience in the following areas:

- AMD design tools
- ModelSim

Available Support Products

To jump-start new designs that combine the Infineon's AURIX microcontrollers with AMD FPGA and adaptive SoC devices and solve the rising safety and performance requirements in emerging automotive and industrial designs, Xylon offers the complete logiHSSL-ZU FPGA HSSL Starter Kit. The kit includes the complete hardware platform built from the AMD Zynq™ UltraScale+™ SoC based ZCU104 Evaluation Kit and the Infineon AURIX Evaluation board with the necessary cabling. Additionally, it comes with the fully functional reference hardware design. To learn more about this product, please contact Xylon or visit our web site:

Email: sales@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHSSL-ZU.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

AMD

For information on AMD programmable logic or development system software, contact your local AMD sales office, or:

Xilinx, Inc.
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Phone: +1 408-559-7778
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Infineon AURIX/TriBoard and HSSL

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Revision History

Version	Date	Note
1.00.	08.05.2019.	Initial Xylon release.
1.01.	07.02.2020.	New physical layer, optimized for AMD FPGAs.
1.02.	15.03.2021.	Removed separate clock for AXI4-Lite Slave. Removed reference clock. Added debug ports. Optimized design.
	16.11.2021.	Updated for Vivado™ 2021.2.
1.02.	15.03.2021.	Removed separate clock for AXI4-Lite Slave. Removed reference clock. Added debug ports. Optimized design.
2.01.	18.07.2024.	Major rewrite of code, starting fom v1.2.3. Removed internal bus, optimized logic, added REDUCE Mode.