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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	
Verification	Thoroughly simulated and hardware validated
Reference Designs & Application Notes	
Additional Items	Standalone SW driver
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports all Xilinx® FPGA families and Zynq®-7000 All Programmable SoC and Zynq® UltraScale+™ MPSoC
- ARM® AMBA® AXI4-Lite bus compliant
- Software programmable I²C clock
- Software programmable Acknowledge bit for read operation
- Interrupt driven data transfer
- Start/repeated start/acknowledge/stop generation
- Supports multi master operation
- Supports clock stretching/wait state generation
- 16 location deep TX and RX data FIFO
- Prepared for Xilinx Vivado® Design Suite (IP Integrator)

Applications

Suitable for embedded designs with Xilinx FPGAs that interface on-board devices (microcontrollers, codecs…) and Xilinx Zynq-7000 AP SoC designs that need more than two I2C interfaces. Example applications include Surveillance, Automotive Driver Assist, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) rclk	LUT[1]	FF[1] (FFs/LUTs)	LUTRAM	IOB[2]	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
Artix®-7 (XC7A35T-2)	180	317	276	16	2	0	0	0	N/A	Vivado 2018.2
Kintex®-7 (XC7K70T-2)	400	321	270	16	2	0	0	0	N/A	Vivado 2017.4
ZYNQ®-7000 (XC7Z010-2)	325	321	270	16	2	0	0	0	N/A	Vivado 2017.4
Zynq® UltraScale+™ (XCZU9EG-1)	325	269	247	16	0	0	0	0	N/A	Vivado 2018.2

Notes:
1) Assuming 32-bit AXI4-Lite register interface.
2) Assuming only I²C signals: SCL and SDA are routed off-chip; register interface and interrupt signal are connected internally.

General Description

The logiI2C is a master I^{2}C bus controller that supports multi-master environment. I^{2}C is a two wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

The interface defines 3 transmission speeds, supported by the logiI2C IP core:

- normal – 100 kbps;
- fast – 400 kbps;
- high speed – 3.5 Mbps.

Functional Description

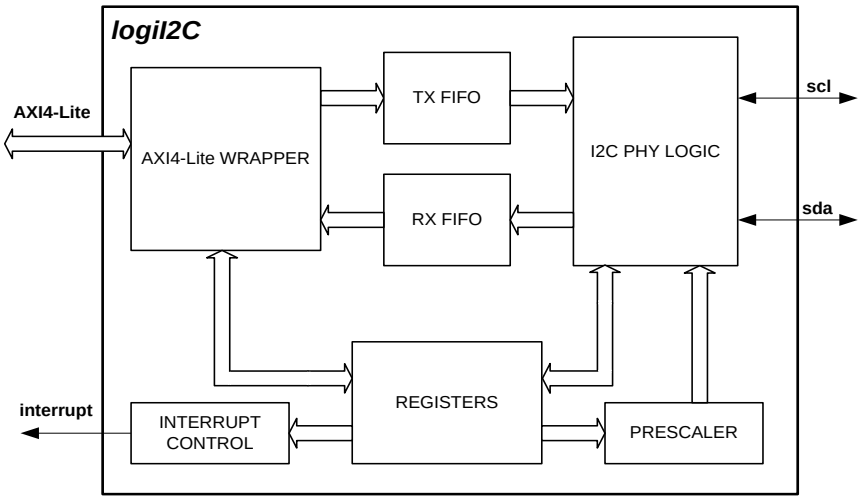

Figure 1: logiI2C Architecture

The Figure 1 presents internal logiI2C IP core architecture. The logiI2C functional blocks are: I2C Phy Logic, TX Data FIFO, RX Data FIFO, AXI4-Lite Wrapper, Registers block, Prescaler and Interrupt Controller.

The I^{2}C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

Phy Logic Block

I2C Phy Logic block contains state machine that handles I^{2}C protocol and generates I^{2}C clock signal.

TX Data FIFO

TX Data FIFO block is 16 locations deep and holds data to be transmitted through the I^{2}C bus. Host CPU writes transmission data along with the stop and the start bits into the FIFO through the AXI4-Lite interface.

RX Data FIFO

RX Data FIFO block is 16 locations deep and holds data received through the I^{2}C bus. Host CPU reads received data from the FIFO through the AXI4-Lite interface.

AXI4-Lite Wrapper

AXI4-Lite Wrapper block is an interface that allows user to access logiI2C registers in the Registers block andthe FIFOs (TX Data FIFO block and RX Data FIFO block) through the AXI4-Lite bus.

Registers

Registers are easily programmed by the host CPU through the AXI4-Lite interface. Therefore, the AXI4-Lite wrapper is included with the logiI2C IP core to provide easy connectivity with processors and other IP cores. All registers are readable.

Prescaler

Prescaler block generates pre-scaled I^2C clock. The pre-scaled clock value is generated from the AXI4-Lite bus clock accordingly to the value programmed into the PRESCAL_REG register. This mechanism enables user to setup the I^2C clock for the specific application.

Interrupt Controller

The Interrupt Controller block generates interrupt signal for the host CPU whenever the corresponding interrupt is enabled and the interrupt condition is satisfied.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with Xilinx Vivado IP Integrator and ISE Platform Studio implementation tools. The logiI2C has configuration parameters that are selectable prior to VHDL synthesis, and the following table presents a selection from a list of available parameters:

Table 2: logiI2C VHDL Configuration Parameters

Parameter	Description
C_REG_BYTE_SWAP	Register access byte swapping option
C_REGS_BASEADDR	Registers base address
C_REGS_HIGHADDR	Registers high address

There may be instances where source code modification is necessary. If you wish to adopt the logiI2C IP core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiI2C IP core to your requirements.

Core I/O Signals

The core signals I/O have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Register Interface		
AXI4-Lite Slave interface	Bus	Refer to ARM's AMBA® AXI4 specification
interrupt	Output	Interrupt output signal, active high, level sensitive
I^2C signals		
sda_i	Input	I^2C serial data – input signal
sda_o	Output	I^2C serial data – output signal
sda_t	Output	I^2C serial data – three state control signal
scl_i	Input	I^2C serial clock – input signal
scl_o	Output	I^2C serial clock – output signal
scl_t	Output	I^2C serial clock – three state control signal

Verification Methods

The logiI2C is fully supported by the Xilinx Vivado Suite. This tight integration tremendously shortens IP integration and verification. A full logiI2C implementation does not require any particular skills beyond general Xilinx tools knowledge. For information about Vivado compatible IP core simulations, please contact Xylon.

The logiI2C evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

URL: www.logicbricks.com/Products/logiI2C.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00.	26.03.2012	Initial Xylon release
1.01.	09.06.2014	Implementation statistics table (Table 1) updated for ISE 14.7
1.1	30.10.2014.	Document updated with information about the Xilinx Vivado compatible logiI2C IP core.
1.1	26.10.2016.	Added utilization information for Zynq® UltraScale+™ XCZU9EG-1 MPSoC. Updated Table 1.
2.0	24.09.2017.	Added multi master support.
	17.10.2018.	Updated implementation statistics table – Table 1