Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design XDC
Verification/Validation	Hardware validated
Reference Designs & Application Notes	On request from Xylon d.o.o.
Additional Items	
Simulation Tool Used	
Mentor Graphics' Modelsim	
Support	
Support provided by Xylon	

Features

- Supports all AMD FPGA families, Zynq®-7000 All Programmable SoC and Zynq UltraScale+™ MPSoC
- Supports up to eight individual I²S instances with the following features:
  - Configurable as receiver or transmitter
  - Configurable as clock master or slave
  - Configurable as word select master or slave
  - Configurable active clock edge
  - Supports three different justification modes: normal (corresponds to the mode specified in the I2S specification by Philips), left and right
  - Configurable TX and RX FIFO depth, from 512 up to 4096 samples (L + R word)
  - Supports word length up to 16 bits
- ARM® AMBA® AXI4-Lite compliant register interface
- Prepared for AMD Vivado® Design Suite (IP Integrator).

Table 1: Example Implementation Statistics for AMD FPGAs

Family (Device)	Fmax (MHz) rclk	LUT[1)]	FF[1)]	IOB[2)]	BRAM	MULT/ DSP48/E	DCM/ CMT	BUFG	GTx	Design Tools
Kintex®-7 (XC7K70T-2)	200	447	548	6	2	-	-	1	N/A	Vivado 2024.1
ZYNQ®-7000 (XC7Z010-2)	200	446	548	6	2	-	-	1	N/A	Vivado 2024.1
Zynq® MPSoC (XCZU9EG- 2L)	200	435	548	6	2	-	-	1	N/A	Vivado 2024.1

Notes:
1) Assuming logiI2S is configured to have one RX and one TX instance, clock and word select masters, normal FIFO size.
2) Assuming only audio inputs and outputs are routed off-chip and register interface is connected internally.

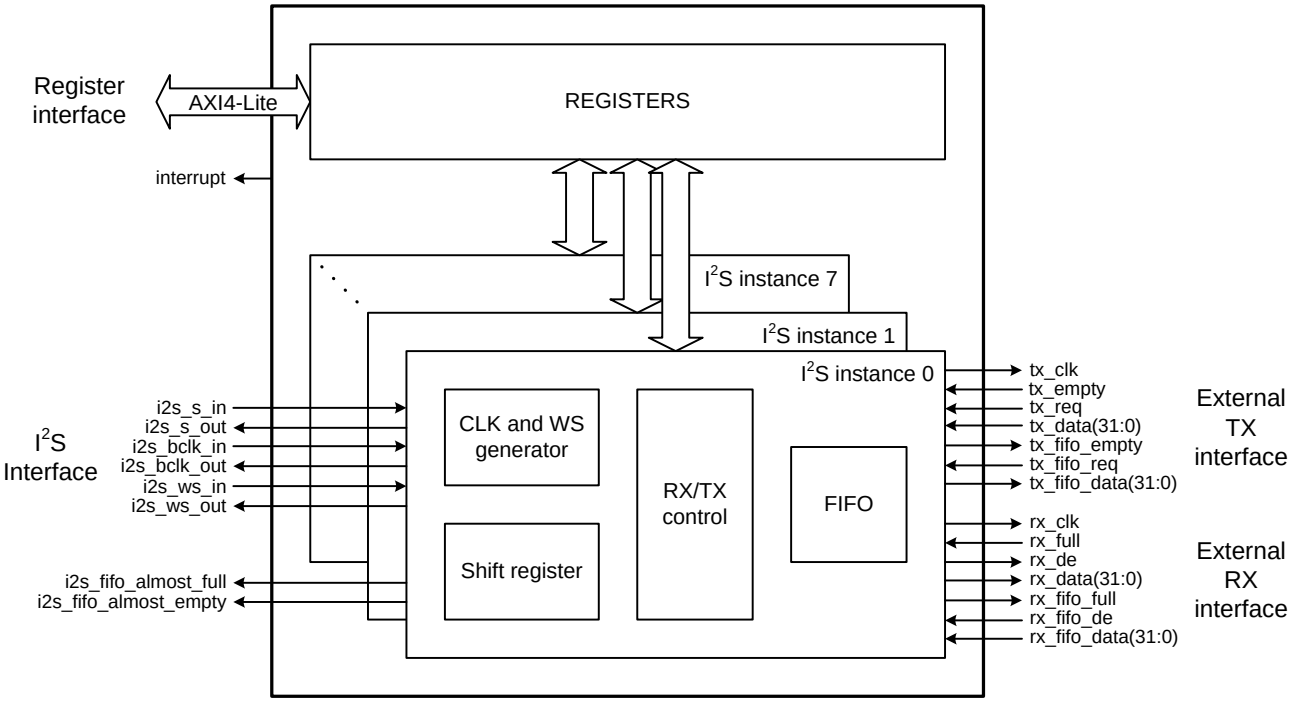

Figure 1: logiI2S Architecture

Applications

Human Machine Interfaces (HMI) for industrial and medical, car infotainment, defense systems, etc.

General Description

The logiI2S is an audio receiver and transmitter IP core from the Xylon logicBRICKS™ IP core library. It enables rapid integration of multi-channel audio functionality in AMD Adaptive Computing devices and supports IP configurations with up to eight I²S transmitters and receivers, stereo audio transport between processors and codecs, configurable clock master and slave modes, etc. The logiI2S IP core is fully embedded into AMD Vivado IP Integrator, and its integration with the on-chip AXI4 bus is very simple. Parametrizable VHDL design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiI2S can be smoothly integrated with other logicBRICKS, AMD or third-party IP cores for building of advanced GUI embedded systems.

Functional Description

The Figure 1 presents internal logiI2S architecture. The logiI2S functional blocks are: I²S Instance and Registers. I²S Instance consists of the Clock and Word select generator, Shift register, TX and RX control logic and FIFO.

I²S Instance

I²S instance can be configured either as an audio receiver or audio transmitter. The I²S instance configured as the audio receiver performs serial to parallel audio data conversion and stores the audio data to RX FIFO. The I²S instance configured as the audio transmitter takes data from TX FIFO and performs parallel to serial audio data conversion.
Additionally, I²S instance supports word length of up to 16 bits per channel, three sample justifications modes, four different FIFO depths, bit clock master or slave and active edge, word select master or slave and invert, left/right channel swap and configurable FIFO almost full/empty flag levels.

Registers

The logiI2S Registers are used for configuration, data streaming and interrupt handling. The logiI2S's register interface is ARM AMBA AXI4-Lite compatible.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with AMD Vivado IP Integrator implementation tools. The logiI2S has configuration parameters that are selectable prior to VHDL synthesis, and the following table presents a selection from a list of available parameters:

Table 2: logiI2S VHDL Configuration Parameters

Parameter[1)]	Description
C_NUM_OF_I2S	Number of I^2S instances (1-8)
C_I2S_**n**_DIRECTION	I^2S instance direction (RX, TX)
C_I2S_**n**_CLOCKMASTER	I^2S instance clock slave or master
C_I2S_**n**_WSMASTER	I^2S instance word select slave or master
C_I2S_**n**_CLOCKEDGE	I^2S instance active clock edge
C_I2S_**n**_WS_INV	I^2S instance word select invert
C_I2S_**n**_LR_SWAP	I^2S instance left/right channel swap
C_I2S_**n**_FIFO_SIZE	I^2S instance FIFO size (512-4096)
C_I2S_**n**_ALMOST_FULL	I^2S instance FIFO almost full level
C_I2S_**n**_ALMOST_EMPTY	I^2S instance FIFO almost empty level
C_I2S_**n**_EXT_INTERFACE	I^2S instance external interface usage

1. n is the number of I^2S instance. Range is from 1 to 8.

There may be instances where source code modification is necessary. If you wish to adopt the logiI2S IP core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiI2S IP core to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal[1)]	Signal Direction	Description
Global Signals		
interrupt	Output	logiI2S interrupt signal, level sensitive, high active
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to ARM AMBA AXI4 specification
I^2S Interface		
i2s_**n**_s_out [2)]	Output	Serial I^2S data output
i2s_**n**_s_in[3)]	Input	Serial I^2S data input
i2s_**n**_bclk_out[4)]	Output	I^2S bit clock output
i2s_**n**_bclk_in[5)]	Input	I^2S bit clock input
i2s_**n**_ws_out [6)]	Output	I^2S word select output
i2s_**n**_ws_in[7)]	Input	I^2S word select input

Signal[1)]	Signal Direction	Description
i2s_**n**_fifo_almost_empty	Output	I^2S FIFO almost empty status
i2s_**n**_fifo_almost_full	Output	I^2S FIFO almost full status
External TX interface		
tx_clk_**n**[2, 8)]	Output	External TX interface clock
tx_empty_**n**[2, 8)]	Input	External TX interface empty input
tx_req_**n**[2, 8)]	Output	External TX interface request output
tx_data_**n**[31:0][2, 8)]	Input	External TX interface data input
tx_fifo_empty_**n**[2, 8)]	Output	External TX interface FIFO empty status
tx_fifo_req_**n**[2, 8)]	Input	External TX interface FIFO request input
tx_fifo_data_**n**[31:0][2, 8)]	Output	External TX interface FIFO data output
External RX interface		
rx_clk_**n**[3, 8)]	Output	External RX interface clock
rx_full_**n**[3, 8)]	Input	External RX interface full input
rx_de_**n**[3, 8)]	Output	External RX interface data enable output
rx_data_**n**[31:0][3, 8)]	Output	External RX interface data output
rx_fifo_full_**n**[3, 8)]	Output	External RX interface FIFO full status
rx_fifo_de_**n**[3, 8)]	Input	External RX interface FIFO data enable input
rx_fifo_data_**n**[31:0][3, 8)]	Input	External RX interface FIFO data input

1. n is the number of I^2S instances. Range is from 1 to 8.
2. Valid only for transmitter I^2S instances
3. Valid only for receiver I^2S instances
4. Valid only when I^2S instance is configured as clock master
5. Valid only when I^2S instance is configured as clock slave
6. Valid only when I^2S instance is configured as word select master
7. Valid only when I^2S instance is configured as word select slave
8. Valid only if generic parameter C_I2S_n_EXT_INTERFACE is set to 1

Verification Methods

The logiI2S is fully supported by the AMD Vivado Suite. This tight integration tremendously shortens IP integration and verification. A full logiI2S implementation does not require any particular skills beyond general AMD tools knowledge. For information about Vivado compatible IP core simulations, please contact Xylon.

The logiI2S evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

URL: www.logicbricks.com/Products/logiI2S.aspx

Recommended Design Experience

The user should have experience in the following areas:

- AMD design tools
- ModelSim

Available Support Products

Xylon provides free pre-verified reference designs to showcase the logiBITBLT graphics accelerator, other Xylon's logicBRICKS 2D and 3D graphics hardware accelerators and display controller IP cores on the most popular AMD Zynq-7000 AP SoC based development kits. Reference designs include evaluation logicBRICKS IP cores and hardware design files, OS image, software drivers, demo applications and documentation.To check a full list of Xylon reference designs please visit the web:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

The logiREF-MEDIA-ZED Human Machine Interfaces pre-verified logicBRICKS reference design showcases the logiI2S audio data receiver/transmitter and other logicBRICKS IP solutions on the ZedBoard kit from Avnet Electronics Marketing.

To download this reference designs, learn more about the design's availability for the ZedBoard development kit, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Multimedia-for-Zynq-AP-SoC-ZedBoard.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

AMD Adaptive Computing

For information on AMD Adaptive Computing or development system software, contact your local AMD sales office, or:

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Revision History

Version	Date	Note
1.00	23.05.2012.	Initial Xylon release – new doc template
1.01	29.06.2012.	Added possibility to independently select master/slave for clock and word select.
2.00	06.12.2012.	Up to eight I^2S TX or RX instances, external interface support, FIFO depth configurable up to 8x, interrupt handling changed (mask and status), almost full and empty configurable per I^2S instance.
2.01	23.01.2013.	Added tx_empty and rx_full signals to the external interfaces.
2.02	09.06.2014.	Data sheet corrections.
2.2	03.12.2014.	New versioning scheme introduced for Vivado packaged IP core.
2.3	21.04.2017.	Added Xilinx Ultrascale/Ultrascale+ architecture support.
	11.04.2019.	Updated Table 1.
	11.04.2025.	Updated document layout. Updated Table 1.