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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Verification/Validation	Simulated and HW validated
Reference Designs & Application Notes	Free reference design (1.3 Mpixel) for the MicroZed™ Embedded Vision Development Kit from Avnet Electronics Marketing
Additional Items	Stand-alone SW driver Bit accurate C Model on request AWB & AE libraries (fee-based license)
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim® Aldec Active-HDL™ and Riviera-PRO™	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, and 7 Series and UltraScale FPGAs
- Complete and configurable ISP pipeline includes:
  - Defective Pixel Correction
  - Color Filter Array Interpolation
  - Image Statistics (+ AWB & AE Support)
  - Color Correction Matrix
  - Gamma Corrections
  - Image Enhancement
  - Motion Adaptive Noise Reduction
  - YCbCr to RGB Color-Space Converter
  - RGB to YCbCr Color-Space Converter
  - Chroma Resampler
- Digitally processes and enhances the quality of an input video stream and collects video statistics data for use in video control algorithms, i.e. Auto White Balance (AWB) and Auto Exposure (AE)
- Supports resolutions up to 7680x7680 including UHD 4K2Kp60 (3840x2160@60fps)
- Supports video input formats: Raw Bayer, RGB and YCbCr; color depth 8/10/12-bit per color
- Parallel pixel processing with configurable number of pixels per clock: 1, 2 or 4
- Video input and output are ARM® AMBA® AXI4-Stream protocol compliant
- Optional registers are AMBA AXI4-Lite protocol compliant
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- Evaluation IP core and bit-accurate C model available on request
- IP deliverables include the software driver, documentation and technical support
- Available fee-based license extension for the AWB&AE libraries, which are verified with the logiISP IP core

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT	FF	IOB	RAMB36	RAMB18	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	aclk	s_axi_clk									
Artix®-7 (XC7A100T-1)	150	196	6531	8197	0	13	10	24	0	0	Vivado 2018.2
Kintex®-7 (XC7K325T-3)	284	303	6586	8197	0	13	10	24	0	0	Vivado 2018.2
Kintex® UltraScale (XCKU040-2)	314	294	6536	8198	0	13	10	20	0	0	Vivado 2018.2

1) Assuming typical configuration: 8bpc, Bayer input, RGB output, 1 pix/clk, AXI4-Lite interface, DPC, CFA, STATS, CCM, GAMMA
2) ENHANCE and MANR blocks can be used in the same configuration as above with additional 5833 LUT, 7555 FF, 10 BRAM, 26 DSP
3) Implementation statistics given for Artix-7 and Kintex-7 FPGAs are also valid for the Zynq-7000 AP SoC family
4) Implementation statistics can vary depending on tool options, other FPGA design logic, speed grade and other

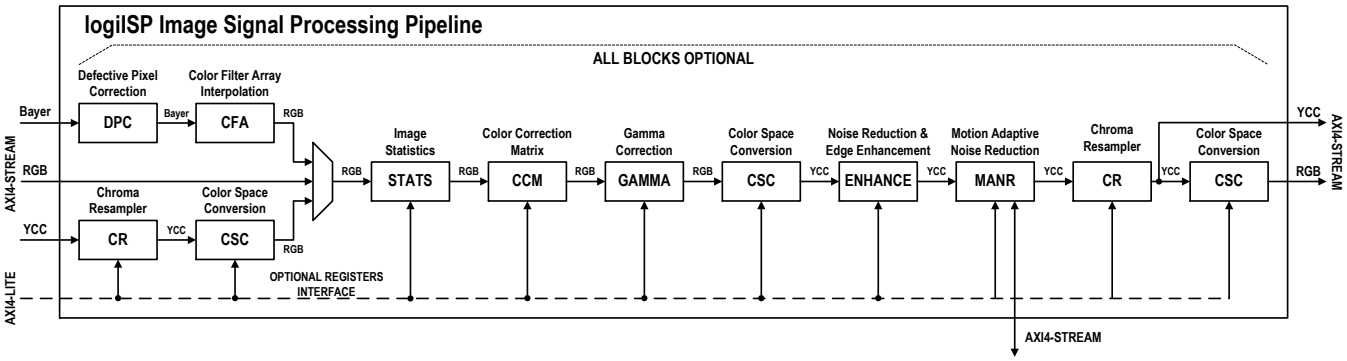

Figure 1: logiISP Architecture

Applications

Application fields include Surveillance, Automotive Driver Assist, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

General Description

The logiISP Image Signal Processing Pipeline IP core is an Ultra High Definition (UHD) ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx Zynq-7000 All Programmable SoC, 7 Series FPGA devices and newer devices.

The logiISP IP core accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data for various control algorithms and manipulates video data formats and color domains. The IP core can be used with processor-based control algorithms for Auto White Balancing (AWB) and Auto Exposure (AE) that work with the video analytics data collected by the ISP pipeline. Xylon offers licensable AWB&AE libraries for the logiISP IP core.

The logiISP IP core supports spatial resolutions up to 7680x7680 including the 4K2Kp60 (3840x2160@60fps) resolution and accepts Raw Bayer, RGB and YCbCr video input formats featuring different pixel color depths (8/10/12-bit per pixel). It outputs RGB or YCbCr formatted processed video and easily adapts to changing image sensor interfaces.

Figures 2 and 3 illustrate video quality enhancements achievable by the logiISP ISP pipeline IP core. The Figure 3 shows the logiISP video output after the processing of the low-quality video input image shown on Figure 2.

Figure 2: Example Video Input Image

Figure 3: Example logiISP Output Image

The logiISP Image Signal Processing Pipeline IP core is prepackaged for Xilinx Vivado IP Integrator (IPI) tool, requires no skills beyond general tools knowledge and can be used in same ways as Xilinx IP cores. Video system designers can easily setup the logiISP ISP pipeline configuration by selecting video input and output formats, switching on and off pipeline stages (blocks) and setting up all IP core's parameters through an easy-to-use IPI GUI interface.

The logiISP IP core is AMBA AXI4 bus protocol compliant and can be smoothly integrated with other Xylon logicBRICKS, Xilinx or third-party IP cores. In combination with other Xylon video and graphics logicBRICKS IP cores, the logiISP can provide the complete end-to-end ISP support from sensor to displayable image.

The logiISP IP core's video input and video output interfaces conform to the AXI4-Stream video protocol and assure low-latency video processing with no need for an external video frame buffering. An optional AXI4-Lite compliant registers interface assures high flexibility and enables processor to fully control the logiISP ISP pipeline, change its settings and use the collected video analytics data, such as the histograms of the data, for processor-based control algorithms.

On request, Xylon provides a bit accurate C model of the logiISP IP core, which is designed for system modeling and quick evaluations with no need for the hardware platform. The logiISP C Model enables users to take an input image, which may be taken from a real camera system, and to get the processed video image equal to the image that would be generated by the logiISP Image Signal Processing Pipeline IP core. In order to get optimal video processing results and to determine appropriate IP core's settings, the user can change and explore different logiISP C Model pipeline configurations and processing parameters.

Besides the logiISP IP core and software driver, Xylon offers consultancy and design services; from the ISP tuning for the specific sensor (camera) up to the full turn-key video processing solutions.

Xylon enables free and risk-free logiISP evaluation on the Xilinx Zynq-7000 AP SoC based MicroZed Embedded Vision Development Kit from Avnet Electronics Marketing. To download and to learn more about the logiREF-VIDEO-ISP-EVK reference design with an integrated logiISP IP core (1 pixel/clock), please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/ISP-Pipeline-for-Xilinx-All-Programmable.aspx

To find more about other evaluation options and learn more about the upcoming High Dynamic Range video processing integration with the Xylon ISP pipeline, please contact info@logicbricks.com.

Functional Description

The Figure 1 presents internal logiISP architecture. The logiISP functional blocks are: Configurable Video Inputs, Defective Pixel Correction, Color Filter Array Interpolation, Chroma Resampler, Color Space Conversion, Image Statistics, Color Correction Matrix, Gamma Correction, Noise Reduction and Edge Enhancement, Motion Adaptive Noise Reduction and logiISP Registers.

Configurable Video Inputs

The logiISP IP core accepts one input formatted as Raw Bayer, RGB or YCbCr (444, 422, 420) video. The receiving logiISP blocks must be selected accordingly.

Defective Pixel Correction (DPC)

The Defective Pixel Correction block performs real-time detection and correction of defective pixels in a camera image sensor array, which may be the result of manufacturing faults, failures during normal operation, or variations in pixel voltage levels based on temperature or exposure. The DPC block detects and repairs defective pixels in the raw Bayer sub-sampled domain.

Color Filter Array Interpolation (CFA)

The Color Filter Array Interpolation block reconstructs sub-sampled color data from images captured by a Bayer Color Filter Array image sensor. Such sensors measure the intensity of one principal color at any pixel location and the CFA block converts them in the RGB formatted video output.

Image Statistics (STATS)

The Image Statistics block implements the computationally intensive metering functionality common in digital cameras, camcorders and imaging devices. The STATS block generates a set of statistics for color histograms, mean and variance values, edge and frequency content for 64 user-defined zones on a per frame basis. The statistical information can be used with different processor-based control algorithms. The Auto-White Balance (AWB) and Auto-Exposure (AE) software libraries can be licensed from Xylon.

Color Correction Matrix (CCM)

The Color Correction Matrix block corrects the image color variations coming from many different causes that can include spectral characteristics of the optics (lens, filters), lighting source variations, characteristics of the color filters of the sensor and many others. The CCM block contains 3x3 programmable coefficient matrix multipliers with offset compensation that can be used in color correction operations such as adjusting white balance, color cast, brightness, or contrast in an image.

Gamma Correction (GAMMA)

The Gamma Correction block manipulates image data to match the non-linear response of display devices. The GAMMA block implements programmable look-up table structures to implement a gamma correction curve transformation. Programmable number of gamma tables enables having separate gamma tables for all color channels or one gamma table shared by all color channels.

Noise Reduction and Edge Enhancement (ENHANCE)

The Noise Reduction and Edge Enhancement block offers noise reduction and/or edge enhancement. For edge enhancement, optional anti-halo and anti-alias post-processing modules are available to reduce image artifacts that can appear from the high-pass filtering of the edge enhancement filters.

Motion Adaptive Noise Reduction (MANR)

The MANR block performs motion adaptive noise reduction in video systems. Noise reduction is used to clean up sensor artifacts or other types of noise present in most video systems. The noise reduction algorithm is implemented as a recursive temporal filter with a user programmable transfer function allowing the user to control both the shape of the motion transfer and the strength of the noise reduction applied.

Color Space Conversion (CSC)

The logiISP IP core features both, RGB to YCbCr and YCbCr to RGB Color-Space Converters. The RGB to YCbCr converter transforms the RGB video data into YCbCr 4:4:4 or YUV 4:4:4 video data. The YCbCr to RGB converter transforms the YCbCr 4:4:4 or YUV 4:4:4 video data into RGB video data. CSC block supports industry standard or user defined conversion matrices.

Chroma Resampler (CR)

The Chroma Resampler block works with the YCbCr video input and converts between different Chroma sub-sampling formats. The supported formats are 4:4:4, 4:2:2 and 4:2:0. CR block supports predefined, power-of-two coefficients for low footprint applications or configurable filter sizes with programmable filter coefficients for high performance applications.

logiISP Registers

The ARM AMBA AXI4-Lite compatible logiISP register interface is optional and can be disabled prior to synthesis. The logiISP IP configured for work with no registers uses hardwired ISP parameters setup through the IPI GUI interface.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with Xilinx Vivado IP Integrator. Many logiISP configuration parameters are selectable prior to VHDL code synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiISP VHDL Configuration Parameters

Parameter	Description
C_ACTIVE_ROWS	Default vertical resolution: 32 – 7680
C_ACTIVE_COLS	Default horizontal resolution: 32 – 7680
C_MAX_COLS	Maximum horizontal resolution: 512, 1024, 2048, 4096, 8192
C_MAX_ROWS	Maximum vertical resolution: 512, 1024, 2048, 4096, 8192
C_S_AXIS_VIDEO_FORMAT	Video input format: Bayer, RGB, YCbCr 444, YCbCr 422, YCbCr 420
C_S_AXIS_VIDEO_DATA_WIDTH	Input Color Data Width: 8, 10, 12-bit
C_S_AXIS_VIDEO_MAX_SAMPLES_PER_CLOCK	Pixels per clock: 1, 2, 4
C_HAS_AXI4_LITE	Enable registers interface: 0, 1
C_HAS_DEBUG	Enable debug module: 0, 1
C_CORE_REGS_READABLE	Enable readability of core specific registers, configurable per block: 0, 1
C_USE_DPC	Enable Defective Pixel Correction block
C_STATUS_WIDTH_DPC	Number of Defective Pixels Tracked
C_THRESH_TEMPORAL_VAR_DPC	Temporal Variance Threshold
C_THRESH_SPATIAL_VAR_DPC	Spatial Variance Threshold
C_THRESH_PIXEL_AGE_DPC	Pixel Age
C_USE_CFA	Enable Color Filter Array Interpolation block
C_BAYER_PHASE_CFA	Bayer Phase
C_HOR_FILT_CFA	Enable Horizontal Zipper Artifact Removal
C_FRINGE_TOL_CFA	Enable Fringe Tolerant or High Resolution Interpolation
C_USE_STATS	Enable Statistics block
C_HAS_RGB_HIST_STATS	Enable RGB histogram
C_HAS_CC_HIST_STATS	Enable CbCr histogram
C_HAS_Y_HIST_STATS	Enable Y histogram
C_HAS_QUANT_Y_HIST_STATS	Enable quantized Y histogram
C_HAS_MAX_MIN_STATS	Enable minimum and maximum
C_HAS_SUM_POW_STATS	Enable sum of color values
C_HAS_EDGE_STATS	Enable edge content
C_HAS_FREQ_STATS	Enable frequency content
C_HAS_PIX_PICKER_STATS	Enable pixel data collection
C_USE_CCM	Enable Color Correction Matrix block
C_Kxy_CCM	Matrix coefficients: x,y ∈ {0, 2}
C_xOFFSET_CCM	RGB Offset: x ∈ {R, G, B}
C_CLIP_CCM	Enable Clipping
C_CLAMP_CCM	Enable Clamping
C_USE_GAMMA	Enable Gamma Correction block
C_LUTS_GAMMA	Number of LUTs
C_INTPOL_GAMMA	Interpolate LUT values
C_DBL_BUF_GAMMA	Enable double buffer LUTs
C_LOAD_INIT_FILE_GAMMA	Load LUT initialization file
C_USE_ENH	Enable Image Enhancement block

Parameter	Description
C_HAS_NOISE_ENH	Enable noise reduction
C_HAS_ENHANCE_ENH	Enable edge enhancement
C_HAS_HALO_ENH	Enable halo suppression
C_HAS_ALIAS_ENH	Enable anti-alias filtering
C_OPT_SIZE_ENH	Implementation quality
C_NOISE_THRESHOLD_ENH	Noise threshold
C_ENHANCE_STRENGTH_ENH	Enhance strength
C_HALO_SUPPRESS_ENH	Halo suppression value
C_YCC_FORMAT_ENH	Enhance input format
C_USE_NOISE	Enable Motion Adaptive Noise Reduction
C_NOISE_REDUCTION	Noise Reduction Strength
C_USE_YCC2RGB	Enable YCbCr to RGB Conversion block
C_xCOEF_YCC2RGB	Conversion coefficients: x ∈ {A, B, C, D}
C_xOFFSET_YCC2RGB	RGB offset compensations: x ∈ {R, G, B}
C_HAS_CLIP_YCC2RGB	Enable output clipping
C_HAS_CLAMP_YCC2RGB	Enable output clamping
C_RGBMAX_YCC2RGB	RGB clipping value
C_RGBMIN_YCC2RGB	RGB clamping value
C_USE_RGB2YCC	Enable RGB to YCbCr conversion
C_xCOEF_RGB2YCC	Conversion coefficients: x ∈ {A, B, C, D}
C_xOFFSET_RGB2YCC	Y, Cb and Cr offset compensations: x ∈ {Y, Cb, Cr}
C_HAS_CLIP_RGB2YCC	Enable output clipping
C_HAS_CLAMP_RGB2YCC	Enable output clamping
C_xMAX_RGB2YCC	Y, Cb and Cr clipping values
C_xMIN_RGB2YCC	Y, Cb and Cr clamping values
C_USE_CRES	Enable Chroma Resample Block
C_CONVERT_TYPE_CRES	Selects between user defined and predefined conversion coefficients
C_NUM_H_TAPS_CRES	Horizontal filter size
C_NUM_V_TAPS_CRES	Vertical filter size
C_CHROMA_PARITY_CRES	Selects chrominance line in 4:2:0 mode

The logiISP is designed with regard to adaptability to various sensors (cameras). However, there may be instances where source code modification is necessary. Therefore, if you wish to adopt the logiISP core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiISP to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Streaming Video Interface		
AXI4-Stream Video Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
AXI4-Stream Video Master Interface	Bus	Refer to Xilinx AXI Reference Guide

Signal	Signal Direction	Description
AXI4-Stream MANR block Master Interface	Bus	Refer to Xilinx AXI Reference Guide
AXI4-Stream MANR block Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
Control Interface		
AXI4-Lite Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
Clock and Reset Signals		
aclk	Input	AXI4-Stream clock, shared between all streaming interfaces
aclken	Input	AXI4-Stream clock enable, shared between all streaming interfaces
aresetn	Input	AXI4-Stream reset, active low, shared between all streaming interfaces
s_axi_aclk	Input	AXI4-Lite clock
s_axi_aresetn	Input	AXI4-Lite reset, active low
Interrupt Interface		
irq	Output	Interrupt request, level sensitive, high active

Verification Methods

The logiISP is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiISP implementation does not require any particular skills beyond general Xilinx tools knowledge.

The logiISP evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logiISP.aspx

Xylon provides a bit accurate logiISP C Model designed for system modeling and quick evaluations with no need for the hardware platform. The logiISP C Model enables users to take an input image, which may be taken from a real camera system, and to get the processed video image equal to the image that would be generated by the logiISP Image Signal Processing Pipeline IP core. The delivery of the logiISP C Model is optional and requires an internal authorization. To learn more about this C model and distribution rules, please contact Xylon:

Email: support@logicbricks.com

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Camera systems

Available Support Products

Xylon provides AWB&AE libraries for use with the logiISP IP core. Please check for the logiREF-VIDEO-ISP-EVK reference design and the provided demo application to evaluate the AWB&AE algorithms. To get more information about this product, please contact Xylon:

Email: support@logicbricks.com

Xylon provides the logiREF-VIDEO-ISP-EVK free pre-verified reference design to showcase the logiISP Image Signal Processing Pipeline IP core on the Xilinx Zynq-7000 AP SoC based MicroZed Embedded Vision Development Kit from Avnet Electronics Marketing. The reference design contains everything you need to

immediately start evaluating and working with the Xylon ISP pipeline: the SoC design including evaluation logicBRICKS IP cores, hardware design files, documentation and the GUI-based demo application (Linux OS):

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/ISP-Pipeline-for-Xilinx-All-Programmable.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	December 1st, 2014	Initial release
1.1	December 9th, 2014	Licensing information changes
1.2	April 23rd, 2015	Added interrupt support. Updated implementation statistics table
1.3	July 6th, 2015	Added new statistic parameters. Updated implementation statistics table
2.0	February 22nd, 2016	Added support for parallel pixel processing.
	September 5th, 2018	Updated implementation statistics table - Table 1