Xylon d.o.o.

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Core Facts

Provided with the Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc examples
Reference Designs & Application Notes	Available for the Xilinx ZC702 kit, please contact info@logicbricks.com
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports AMD-Xilinx Zynq®-7000 SoC, Zynq UltraScale+™ MPSoC and 7 series FPGAs
- Losless on-the-fly video decoder of Motion JPEG (MJPEG) video stream
- Compliant with the Annex H of the ISO/IEC 10918-1 JPEG standard
- Lossless process based on the Huffman coding algorithm. Video input/output resolutions up to 4096x16384
- Typical speed in mid-range FPGAs is 150 MPix/s when running at 150MHz, 1 pixel/clock processing
- ARM® AMBA® AXI4-Stream-compliant input: accepts lossless JPEG frame-by-frame , decompresses it and provides a decompressed video frame at the AMBA AXI4-Stream-compliant video output
- Output can be used as a video stream for additional on-chip video processing or stored to memory with any AXI Video DMA engine.
- The IP core supports loslessly encoded JPEG input frames (JPEG LS) with one color component only and precision up to 12 bits. This is used in applications where multicolor-component video is compressed separately for each color plane; one JPEG LS frame for one color component.
- Full color JPEG frames divided into multiple color planes can be decompressed sequentially, color by color plane, or in parallel by multiple logiJPEG-LS IP core instances
- For optimal FPGA utilization, should be configured to work with the fixed Huffman table
- For more flexibility, should be configured to use the Huffman table from the input JPEG header
- Keeps up the exact frame rate to ensure smooth playback of Motion JPEG encoded video
- Automatic parsing of JPEG markers and recovery from the error state (invalid marker recognition)
- No-programming required; a single control signal input enables/disables the AXI4-Stream MJPEG output

Table 1: Example Implementation Statistics for AMD-Xilinx FPGAs

Family (Device)	Fmax (MHz) clk	LUT	FF	IOB	BRAM	DSP48	PLL/ MMCM	BUFG/ BUFR	GTx	Design Tools
Zynq-7000 (XC7Z020-1)	150	1628	561	0	4	0	0	0	0	Vivado 2021.1
Artix®-7 (XCA200T-2)	220	1772	561	0	4	0	0	0	0	Vivado 2021.1
Kintex®-7 (XC7K325T-2)	220	1667	561	0	4	0	0	0	0	Vivado 2021.1

1) Assuming the following configuration: minimal horizontal resolution 2048, vertical resolution up to 16K (in compliance with the standard), maximal precision 12 bit

- Parametrical VHDL design that allows tuning of slice consumption and features set
- Available IP core deliverables prepared for the Xilinx Vivado® Design Suite 2021.1

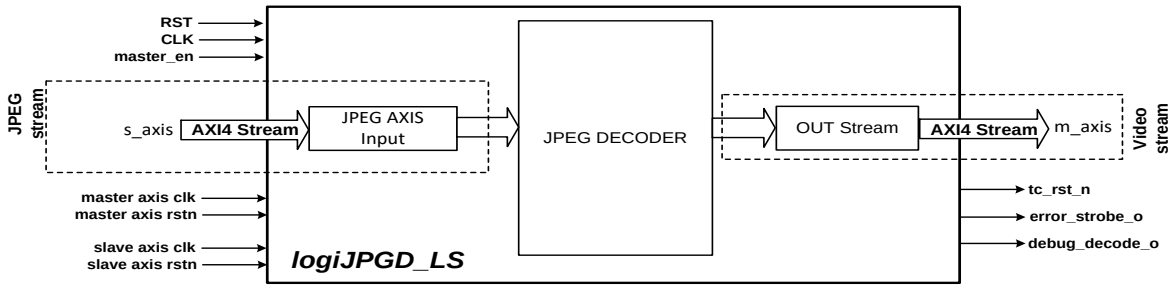

Figure 1 logiJPGD-LS IP Core' Architecture

- IP deliverables include documentation and technical support
- Plug and Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, such as the logiJPGE-LS Lossless MJPEG encoder and the logiISP Image Signal Processing Pipeline

Applications

The logiJPGD-LS IP core can be used in all applications that require JPEG Lossless video decompression. It is particularly well-suited for video over IP applications such as:

- Various cameras
- Automotive Multi-Camera Computer vision ADAS/AD systems
- Multi-camera surveillance systems
- Data logging devices

General Description

The logiJPGD-LS Motion JPEG (MJPEG) Decoder is Xylon's logicBRICKS IP core for still image and video decompression applications on AMD-Xilinx MPSoC, SoC, and FPGA devices. It includes all logic blocks necessary for quick implementations of ARM AMBA AXI4 streaming-based FPGA/SoC architectures and enables on-the-fly JPEG decompression of input video with resolutions up to 4096x16384 (including full HD video at 60 fps – 1080p@60).

At the center of the logiJPGD-LS IP core is a decoder block, based on the Huffman coding algorithm. It works with the color component precision up to 12 bits and supports standard JPEG headers. The JPGD-LS decoder block is coupled with the Slave AMBA AXI4-Stream input data bus that handles input JPEG LS frames. The logiJPGD-LS outputs the de-compressed video output data via Master AXI4-Stram video output data bus towards next stages in the video processing pipeline.

logiJPGD-LS supports decompression of JPEG LS frames with one color component only, the so-called color plane. A full multi-color video decompression requies division of JPEG encoded multi-color videos (i.e. Bayer, YUV, RGB) in separated JPEG LS frames per color component – color planes. One logiJPGD-LS IP core can sequentially decompress all color planes to generate multi-color video output. Alternatively, multiple logiJPGD-LS IP cores instantiated in a parallel can decompress all input color planes at once.

In typical IP applications, a previously encoded (compressed) MJPEG video is decoded (de-compressed) and transferred to the IP core's output. The de-compressed video can be further processed by the next block in the video pipeline, or with an additional Xilinx IP such as AXI Video DMA, directly stored to off-chip

memory. The logiJPGD-LS IP core works smoothly with Xylon's logiJPEG-LS encoder IP core, as well as all other lossless MJPEG encoders compatible with the Annex H of the ISO/IEC 10918-1 JPEG standard.

A variety of interrelated factors affect the achievable logiJPGD-LS IP core's performance. The targeted Xilinx programmable device, the overall FPGA/SoC design's complexity and the input video resolutions and frame rates are the most important parameters that affect an IP core's performance.

The logiJPGD-LS is fully embedded into Xilinx Vivado IP implementation tools, hides complexity from the end user, and its integration with the on-chip AMBA AXI4-Stream bus is easy. It does not need any initialization and software support, and it works even in systems without a CPU. Parametrizable VHDL design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiJPGD_LS can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores.

If you are interested in the logiJPGD-LS MJPEG Decoded IP Core's evaluation, please contact info@logicbricks.com or visit https://www.logicbricks.com/Products/logiJPGD-LS.aspx.

Application Example

Because of their high performance that enables real-time video compression/decompression of high resolution video, lossless algorithms that prevent unwanted artifacts in video recordings used validation of computer vision-based ADAS/AD systems, Machine Learning and AI check-up, and extremely efficient and small footprint in programmable logic, the logiJPGE-LS MJPEG encoder and the logiJPGD-LS MJPEG decoder are used in Xylon's logiRECORDER Automotive HIL Video Logger. The video compression/decompression IP pair is integrated in the video I/O module's AMD-Xilinx FPGA. Quality video compression enables storage of longer video recordings on available disks' storage space, while the embedded video decoders enable an immediate playback of decompressed video generated from locally stored compressed video recordings.

To find out more about the logiRECORDER, visit: https://xylon-lab.com/product/logirecorder/

Figure 2 Video Module for Xylon's logiRECORDER

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado Design Suite (IP Integrator), which allows the user to take full control over IP configuration parameters. Table 2 outlines several important logiJPGD_LS configuration parameters selectable prior to the VHDL synthesis.

Table 2: logiJPGD-LS Configuration Parameters

Parameter	Description
C_MAX_H_RESOLUTION	Maximum horizontal resolution: 512 to 4096. Maximal vertical resolution is defined by JPEG standard: 64k llines
C_USE_CALC_HUFF_TABLE	Defines the Huffman table used for decoding: 0 – Use fixed Huffman table 1 – Use Huffman table from JPEG header

Parameter	Description
C_TIMEOUT_REG	Output stall terminate counter timeout. 332 ms @ 150 MHz

The logiJPGD-LS has been constructed with regard to adaptability to various video applications. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach the optimal use of the logiJPGD-LS core and/or to implement some of your specific functions, you can order the source code or allow us to tailor the logiJPGD-LS to your requirements. The logiJPGD-LS VHDL source code is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in **Error! Reference source not found.**.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
rst	Input	Global reset input
clk	Input	Main clock input
Streaming Interface		
S_AXIS AXI4-Stream Interface	Bus	Input ARM AMBA AXI4-Stream slave interface
M_AXIS AXI4-Stream Video Interface	Bus	Output ARM AMBA AXI4-Stream master video interface
Auxiliary Signals		
master_en	Input	Decode Processing Enable signal
error_strobe_o	Output	Signal indicationg various type of errors during decoding. 0 – Bad precision or bad component 1 - Bad height or bad width or bad SOF length or start reset 2 – Huffman table init error 3 – Unexpected marker error 4 – Error detected while decoding unknown Huffman symbol 7 – 5 – Not used (zeroes)
tc_rst_n	Output	Timeout reset signal

Verification Methods

The logiJPGD-LS is fully supported by the Xilinx Vivado Design Suite 2021.1. This tight integration tremendously shortens IP integration and verification. The logiJPGD-LS has already been used in automotive production systems and its full implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiJPGD-LS MJPEG Decoder can by paired by the logiJPGE-LS MJPEG Encoder IP core from the logicBRICKS by Xylon® IP cores library. To learn more about this IP core, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiJPGD-LS.aspx

Ordering Information

This product is available directly from Xylon under the terms of Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.03	24.02.2022	Initial

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