Xylon d.o.o.

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Core Facts

Provided with the Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc examples
Reference Designs & Application Notes	Available for the Xilinx ZC102 evaluation kit, please contact info@logicbricks.com
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports AMD-Xilinx Zynq®-7000 SoC, Zynq UltraScale+™ MPSoC and 7 series FPGAs
- Lossless on-the-fly video encoder to Motion JPEG (MJPEG) video stream
- Compliant with the Annex H of the ISO/IEC 10918-1 JPEG standard
- JPEG markers inserted on-the-fly in the compressed output stream
- Lossless process based on the Huffman coding algorithm. Video input/output resolutions up to 4096x16384
- Typical speed in mid-range FPGAs is 150 MPix/s when running at 150MHz, 1 pixel/clock processing
- ARM® AMBA® AXI4-Stream-compliant video input: accepts video frame-by-frame, compresses it and provides a compressed lossless JPEG frame at the AMBA AXI4-Stream-compliant output
- The IP core supports video input frames with one color component only and precision up to 12 bits. This is used in applications where multicolor-component video is encoded separately for each color plane; one JPEG LS frame for one color component.
- Full color video frames divided into multiple color planes can be compressed sequentially, color by color plane, or in parallel by multiple logiJPGE-LS IP core instances
- No-programming required; a single control signal input enables/disables the AXI4-Stream MJPEG output
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Available IP core deliverables prepared for the Xilinx Vivado® Design Suite 2021.1
- IP deliverables include documentation and technical support
- Plug and Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiJPGE-LS Lossless MJPEG encoder and the logiISP Image Signal Processing Pipeline

Table 1: Example Implementation Statistics for AMD-Xilinx FPGAs

Family (Device)	Fmax (MHz) clk	LUT	FF	IOB	BRAM	DSP48	PLL/ MMCM	BUFG/ BUFR	GTx	Design Tools
Zynq-7000 (XC7Z020-1)	150	1341	1231	0	0	0	0	0	0	Vivado 2021.1
Artix®-7 (XCA200T-2)	220	1347	1237	0	0	0	0	0	0	Vivado 2021.1
Kintex®-7 (XC7K325T-2)	220	1345	1232	0	0	0	0	0	0	Vivado 2021.1

1) Assuming the following configuration: minimal horizontal resolution 2048, vertical resolution up to 16K (in compliance with the standard),

- IP deliverables include documentation and technical support
- Plug and Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiJPGE-LS Lossless MJPEG encoder and the logiISP Image Signal Processing Pipeline

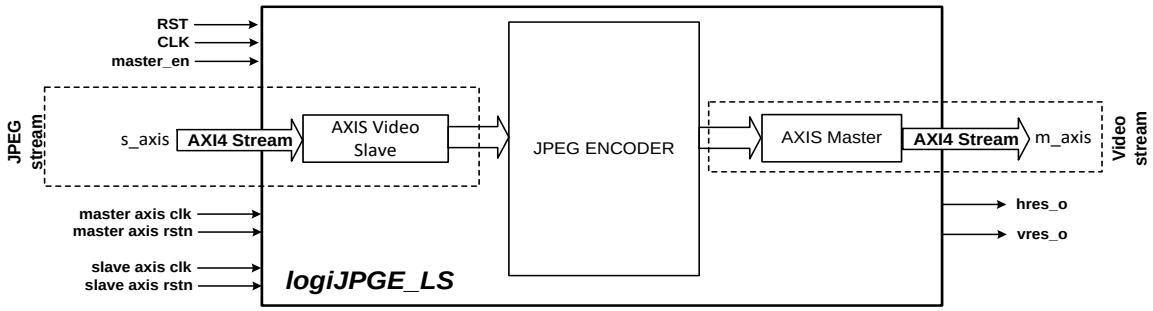

Figure 1 logiJPGE-LS IP Core Architecture

Applications

The logiJPGE-LS IP core can be used in all applications that require JPEG Lossless video compression. It is particularly well-suited for video over IP applications such as:

- Various camera designs with an integrated video compression feature
- Automotive Multi-Camera Computer vision ADAS/AD systems
- Multi-camera surveillance systems
- Data logging devices

General Description

The logiJPGE-LS Motion JPEG (MJPEG) Lossless Encoder is Xylon's logicBRICKS IP core for still image and video compression applications on AMD-Xilinx MPSoC, SoC and FPGA devices. It includes all logic blocks necessary for quick implementations of AMBA AXI4 streaming-based FPGA/SoC architectures and enables on the fly JPEG compression of input video with resolutions up to 4096x16384 (including full HD video at 60 fps – 1080p@60).

At the center of the logiJPGE-LS IP core is an encoder block that works with the color component precision up to 12 bits and utilizes standard JPEG headers on the output stream. The JPEG-LS encoder block is coupled with the Slave AMBA AXI4-Stream input bus that handles video data from the video source. The logiJPGE_LS outputs compressed video data via Master AXI4-Stream output data bus towards next stages in the video processing pipeline.

logiJPGE-LS supports compression of video input frames with one color component only, the so-called color plane. A full multi-color video compression requires division of input multi-color videos (i.e. Bayer, YUV, RGB) to separated frames per color component – color planes. One logiJPGE-LS IP core can sequentially compress all color planes to generate multi-color JPEG LS output. Alternatively, multiple logiJPGE-LS IP cores instantiated in parallel can compress all input color planes at once.

In typical IP applications, input video stream is encoded (compressed) MJPEG and transferred to the IP core's output. Compressed video can be further processed by the next block in the pipeline, or with an additional Xilinx IP such as AXI DMA, directly stored to off-chip memory. The logiJPGE-LS IP core works smoothly with Xylon's logiJPGD-LS decoder IP core, as well as all other lossless MJPEG decoders compatible with the Annex H of the ISO/IEC 10918-1 JPEG standard.

A variety of interrelated factors affect the achievable logiJPGE-LS IP core's performance. The targeted AMD-Xilinx programmable device, the overall FPGA/SoC design's complexity and the input video resolutions and frame rates are the most important parameters that affect a core's performance.

The logiJPGE-LS is fully embedded into Xilinx Vivado IP implementation tools, it hides complexity from the end user, and its integration with the on-chip AMBA AXI4-Stream bus is easy. It does not need any initialization and software support and it works even in systems without a CPU. Parametrizable VHDL design allows for tuning of slice consumption and features set through an easy-to-use GUI interface. The logiJPGE_LS can be smoothly integrated with other logicBRICKS, Xilinx or third-party IP cores.

If you are interested in the logiJPGE-LS MJPEG Encoder IP Core's evaluation, please contact info@logicbricks.com or visit https://www.logicbricks.com/Products/logiJPGE-LS.aspx.

Application Example

Because of their high performance that enables real-time video compression/decompression of high resolution video, lossless algorithms that prevent unwanted artifacts in video recordings used validation of computer vision-based ADAS/AD systems, Machine Learning and AI check-up, and extremely efficient and small footprint in programmable logic, the logiJPGE-LS MJPEG encoder and the logiJPGD-LS MJPEG decoder are used in Xylon's logiRECORDER Automotive HIL Video Logger. The video compression/decompression IP pair is integrated in the video I/O module's AMD-Xilinx FPGA. Quality video compression enables storage of longer video recordings on available disks' storage space, while the embedded video decoders enable an immediate playback of decompressed video generated from locally stored compressed video recordings.

To find out more about the logiRECORDER, visit: https://xylon-lab.com/product/logirecorder/

Figure 2 Video Module for Xylon's logiRECORDER

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado Design Suite (IP Integrator), which allows the user to take full control over IP configuration parameters. Table 2 outlines several important logiJPGE-LS configuration parameters selectable prior to the VHDL synthesis.

Table 2: logiJPGE-LS Configuration Parameters

Parameter	Description
C_MAX_HRES	Maximum horizontal resolution: 512 to 4096. Maximal vertical resolution is defined by JPEG standard: 64k llines
C_M_AXIS_TDATA_WIDTH	Output Data Width: 8b or 16b

The logiJPGE-LS has been constructed with regard to adaptability to various video applications. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach

the optimal use of the logiJPGE-LS core and/or to implement some of your specific functions, you can order the source code or allow us to tailor the logiJPGE-LS to your requirements. The logiJPGE-LS VHDL source code is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
rst	Input	Global reset input
clk	Input	Main clock input
Streaming Interface		
S_AXIS AXI4-Stream Interface	Bus	Input ARM AMBA AXI4-Stream slave interface
M_AXIS AXI4-Stream Video Interface	Bus	Output ARM AMBA AXI4-Stream master video interface
Auxiliary Signals		
master_en	Input	Encode Processing Enable signal
hres	Input	Input frame Horizontal resolution
vres	Input	Input frame Vertical Resolution
hres	Output	Output frame Horizontal resolution
vres	Output	Output frame Vertical Resolution

Verification Methods

The logiJPGE-LS is fully supported by the Xilinx Vivado Design Suite 2021.1. This tight integration tremendously shortens IP integration and verification. The logiJPGE-LS has already been used in automotive production systems and its full implementation does not require any particular skills beyond general Xilinx tools knowledge

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiJPGE-LS MJPEG Encoder can be paired with the logiJPGD-LS MJPEG Decoder IP core from the logicBRICKS by Xylon® IP cores library. To learn more about this IP core, contact Xylon or visit the web:
Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiJPGE-LS.aspx

Ordering Information

This product is available directly from Xylon under the terms of Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.03	24.02.2022	Initial