Core Facts

Provided with Core	
Documentation	logiLENS User's Manual, logiLENS Calibration Software User's Manual
Design File Formats	encrypted VHDL
Constraints Files	logiLENS.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	Reference EDK design
Additional Items	logiLENS calibration software HW platform logiCRAFT2 HW platform logiCRAFT3 Xilinx XtremeDSP Video Starter Kit — Spartan-3A DSP Edition
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support Provided by Xylon	

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Features

- Available under terms of the SignOnce IP License
- Supports real-time correction of video distorted by video camera + lens system
- Removes various distortion types, i.e. fish-eye, barrel, pincushion
- Designed for interfacing configurable (32 or 64 bits) Xylon logiMEM and Xilinx MPMC memory controllers. Other memory bus interfaces can be supported on request
- Does not require external SRAM for storage of intermediate results; the corrected video stores directly to frame buffers implemented in SDR/DDR SDRAM or SRAM
- User friendly and easy-to-use logiLENS calibration software with result preview function
- The calibration software generates VHDL package file or header file containing data configured for specific lens and camera system
- Supports input resolutions up to 1024 x 512pixels
- Supports output resolutions up to 2048 x 1024
- Output image cropping and positioning

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices[1]	IOB[2]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Spartan®-3E	XC3S1200-5	127	2125	209	1	16	12	0	N/A	ISE® 10.1.03i
Spartan®-3A	XC3SD1800A-5	130	2124	209	1	16	12	0	N/A	ISE® 10.1.03i
Virtex®-4	XC4VFX12-12	205	2142	209	1	16	12	0	N/A	ISE® 10.1.03i
Virtex®-5	XC5VLX30-3	240	926	209	1	16	12	0	N/A	ISE® 10.1.03i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

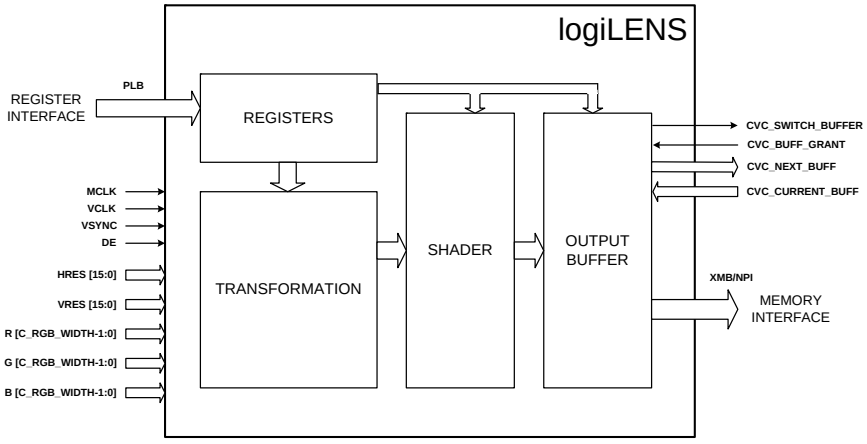

Figure 1: logiLENS Block Diagram

Features (continued)

- Works with streaming or stopped video
- Configurable pixel row stride
- An optional register interface compatible to Xilinx (IBM) PLBv46. The logiLENS can be configured for particular lens and work without register interface
- Quadruple buffering prevents video flickering
- Supports distortion correction for wide variety of lenses with up to 180° Field Of View (FOV)
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Prepared for Xilinx Platform Studio (XPS) and the EDK
- Plug'n'play with other Xylon logicBRICKS™ IP cores like logiCVC-ML Compact Video Controllers, logiMEM flexible SDR/DDR Memory controller and logiBAYER Bayer pattern demosaicing

Applications

- Automotive rear-view camera
- Surveillance camera systems
- Consumer digital cameras

General Description

The logiLENS is an IP core, from Xylon logicBRICKS™ IP library, optimized for Xilinx FPGAs and designed to process video data stream captured by video cameras. The video cameras can be equipped with lenses that may advertently or inadvertently distort the captured video, and those distortions can be corrected and removed by the logiLENS. Example of an application using advertently distorted video is the automotive rear-view camera, which gains a wide adoption as one of the most popular Driver Assistance Systems (DAS). The rear-view camera uses wide or eye-fish lens to capture wide scene behind the vehicle. The distorted captured video must be rectilinearly projected on flat LCD display to aid driver in backing up. The rectilinear projection requires real-time execution of complex mathematical algorithms that calculate corrected video picture. The logiLENS is being designed to support such video processing.

The logiLENS IP core comes with the logiLENS calibration software that enables a preview feature. The logiLENS user can setup particular video system by parameters selected and checked by the calibration preview. The software supports a wide variety of lenses and output image resolutions. The selected

system parameters are automatically packed into VHDL package file or C header file. The configuration files present a valuable aid in system programming.

The logiLENS accepts standard 24-bit RGB video input. The IP is internally pipelined and does not require memory storage of intermediate calculation results. It stores a fully corrected video into frame buffers implemented in SDRAM memories out of the Xilinx FPGA chip.

The FPGA interfaces external memory chips by mean of FPGA implemented memory controller. The logiLENS currently supports interfaces towards Xylon logiMEM and Xilinx MPMC multi-ported memory controllers. The logiLENS efficiently utilizes memory interface and, in comparison to undistorted RGB video input, ads a modest bus overload (about 15%) caused by the internal pipelining.

The Figure 2 presents a block diagram of demo FPGA design for Xylon Evaluation/Development platform logiCRAFT2, based on several Xylon logicBRICKS™ and Xilinx IP cores. Xylon's logiCVC-ML multi-layered versatile video controller displays corrected camera video as a layer on the LCD display. This layer can be overlaid (blended, color keyed, etc.) by other display's layers showing computer generated still graphics, animations, or even other video streams.

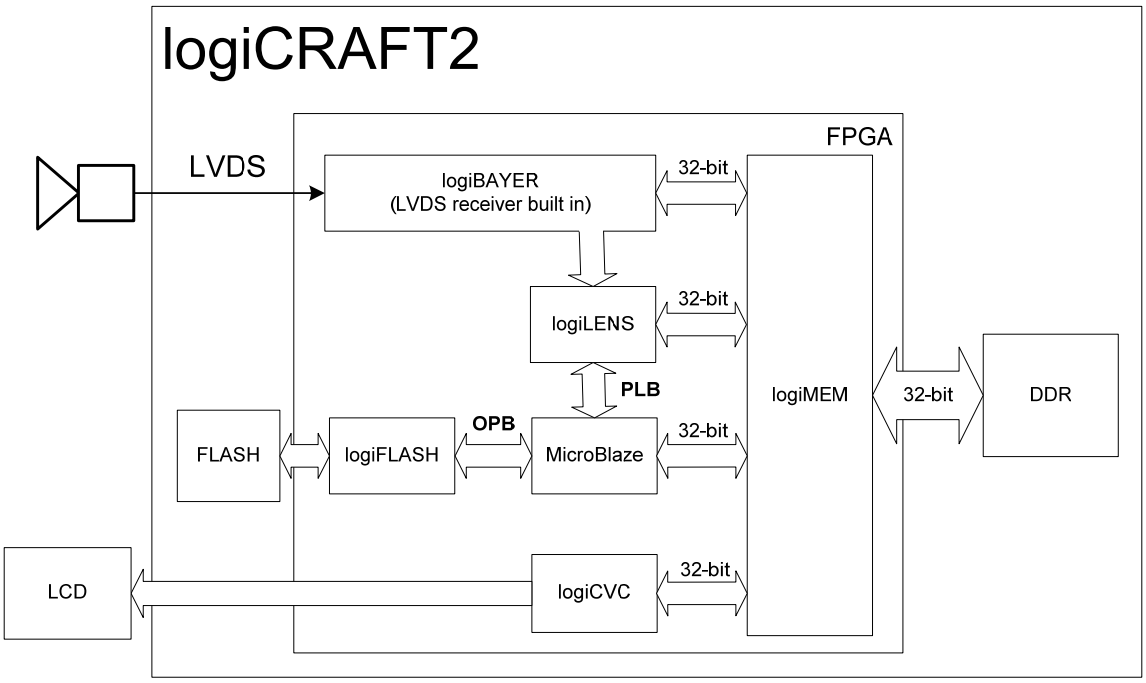

Figure 2: logiLENS Reference design

Functional Description

The Figure 1 presents an internal logiLENS architecture. The logiLENS functional blocks are: Transformation, Shader, Output buffer with memory interface, and an optional registers block.

TRANSFORMATION

The Transformation block uses multiple BRAM instances for input video capture. Positions of video pixels in undistorted space are calculated from positions of pixels stored in the input BRAMs. Newly calculated pixel positions and color information go to a next processing block in the logiLENS pipeline.

SHADER

The Shader accepts Transformation block's outputs and efficiently calculates two missing pixels per each clock cycle. Resulting Shader's output in undistorted video with color information that go to IP's Output buffer block.

OUTPUT BUFFER

The Output Buffer executes a final pixels processing and packs logiLENS output data into output BRAMs. The Shader's output can have multiple pixels with an equally calculated position within the undistorted space and their color information must be averaged prior to memory storage. The output BRAMs are emptied accordingly to an algorithm developed to exploit SDRAM memory bursts and quadruple frame buffers.

REGISTERS

The register interface is an optional block. It allows you to change logiLENS parameters by software and in a real time. The registers' PLB wrapper enables an easy interconnection with the Xilinx MicroBlaze and PowerPC processors.

Core Modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. Many logiLENS configuration parameters are selectable prior to VHDL synthesis, and the following table presents the most important parameters:

Table 2: logiLENS VHDL configuration parameters

Parameter	Description
C_REGS_INTERFACE	Selects registers enabling real time cropping, positioning, etc., or a package file for fixed logiLENS configuration without registers
C_VMEM_INTERFACE	XMB (Xylon memory bus) or NPI (Xilinx MPMC) interface to memory, variable memory data width: 32 or 64-bit
C_MULT_BUFFERING	Quadruple buffering on/off; row stride and buffer offset in number of lines can be chosen

The logiLENS has been designed with regard to adaptability to various cameras. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiLENS core or to supplement some of your specific functions, you can allow us to tailor the logiLENS to your requirements.

Core I/O Signals

The core signal I/O has not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals.

Signal	Signal Direction	Description
Global signals		
RST	Input	Global synchronous set/reset
VCLK	Input	Video Input Clock
MCLK	Input	Video Memory Clock

Memory interface		
XMB Interface	Bus	Xylon Memory Bus. Refer to Xylon logiMEM specifications
NPI Interface	Bus	Xilinx Multi Port Memory Controller. Refer to Xilinx MPMC specifications
Register interface		
PLBV46 Slave Interface	Bus	Refer to Xilinx-IBM CoreConnect specifications
Auxiliary signals		
VSYNC	Input	Vertical synchronization
DE	Input	Data enable (line valid)
HRES	Input	Horizontal resolution
VRES	Input	Vertical resolution
R(C_RGB_WIDTH - 1 downto 0)	Input	Red component of video input data
G(C_RGB_WIDTH - 1 downto 0)	Input	Green component of video input data
B(C_RGB_WIDTH - 1 downto 0)	Input	Blue component of video input data
CVC_switch_buffer	Output	Switch video buffer (used for quadruple buffering), active at the beginning of frame
CVC_buff_grant	Input	Switch video buffer granted (used for quadruple buffering)
CVC_current_buff	Output	Current video buffer (used for quadruple buffering)
CVC_next_buff	Input	Next video buffer (used for quadruple buffering)

Verification Methods

The logiLENS is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiLENS implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on logiCRAFT2 and logiCRAFT3 Xylon development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. Both platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. The platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: info@logicbricks.com
URL: www.logicbricks.com/html/evaluation_boards.htm

Ordering Information

This product is available directly from Xylon under the terms of the SignOnce IP License. Please contact Xylon for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Xylon or visit the web:

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Related Information

Xilinx Programmable Logic

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