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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Verification	Reference design simulation
Reference Designs & Application Notes	Vivado reference design
Additional Items	SW drivers, API and post-processing library
Simulation Tool Used	
Vivado Simulator	
Support	
Support provided by Xylon	

Features

- Fundamental building block for FPGA-based Rear Looking Lane Departure Warning System
- Supports Xilinx® Zynq®-7000 and Xilinx® Zynq®-UltraScale+ Xilinx FPGAs
- Uses a simple, robust and fast lane model based on straight quasi-vertical lines
- Adapts to shadows and light changes
- Hough Transform based model fitting
- Implements the most computing demanding tasks in programmable logic
- Provides high level decision making reasoning as open source embedded software
- ARM® AMBA® AXI4 compliant Memory Mapped Register Interface
- AXI4 Slave Stream Video Input Interface
- High Input Data rate; > 200 Mpixel/sec
- Customizable input image dimension (default 800x600)
- Supports RGB(8:8:8), YUV(4:4:4) and YUV(4:2:2) video stream format
- Vivado reference design including demo software application
- C code post-processing library available

Applications

- Driver Assistance Systems

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) Sysgen_clk	LUTs	FFs	IOB	CMT	BRAM[2]	DSP48A	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z020-1)	100	2,893	4,147	0	0	13	15	0	N/A	Vivado 2018.2
Zynq®-UltraScale+ (XCZU9EG-2)	100	2,875	4,147	0	0	13	15	0	N/A	Vivado 2018.2

1) Assuming configuration with default IP parameters (including Selector and DrawLines blocks)

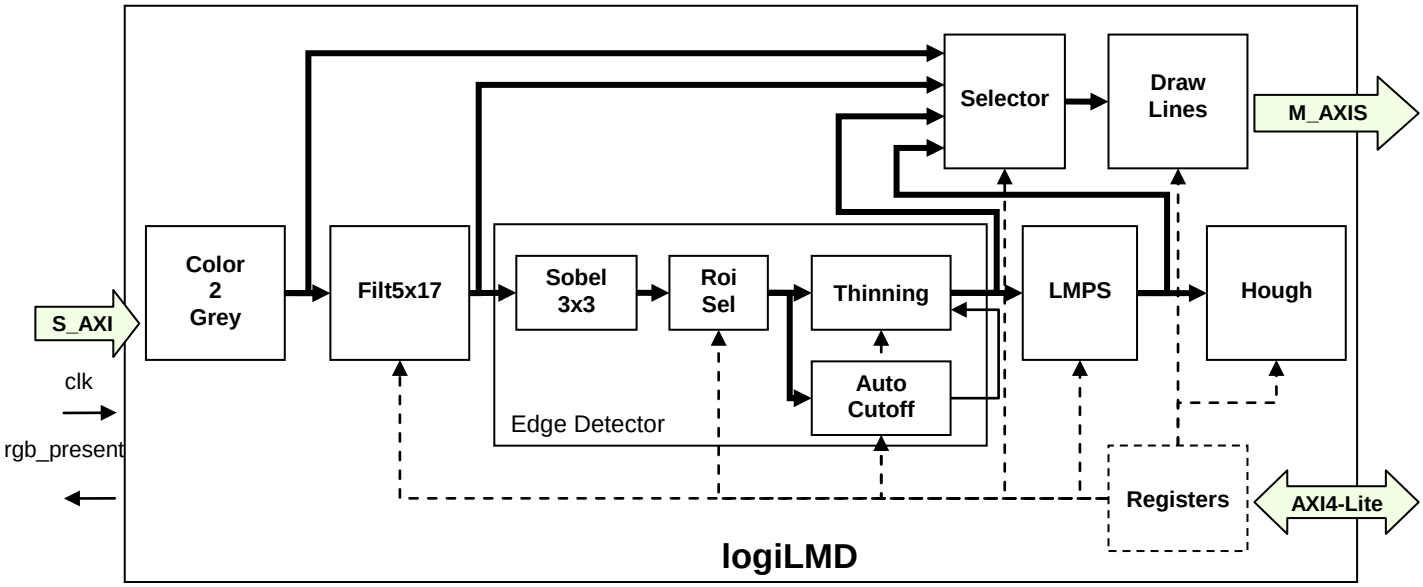

Figure 1: logiLMD Architecture

General Description

Lane Departure Warning Systems (LDWS) are typically electronic automotive systems that indentify and track the markings corresponding to the lane boundaries, locate the vehicle position with respect to them and issue a warning when the vehicle crosses the lane bounds.

The logiLMD Lane Marking Detection IP core from Xylon's logicBRICKS IP core library is designed to detect the lane markings on the roadway video scenarios captured from a rear view camera and to raise an issue in case the host's vehicle departs from the lane. Its functions include image-processing filters, like Gaussian smoothing and Edge detection, and blocks specifically tailored for lane marking detections. The output of the core is the set of straight lines corresponding to lane markings.

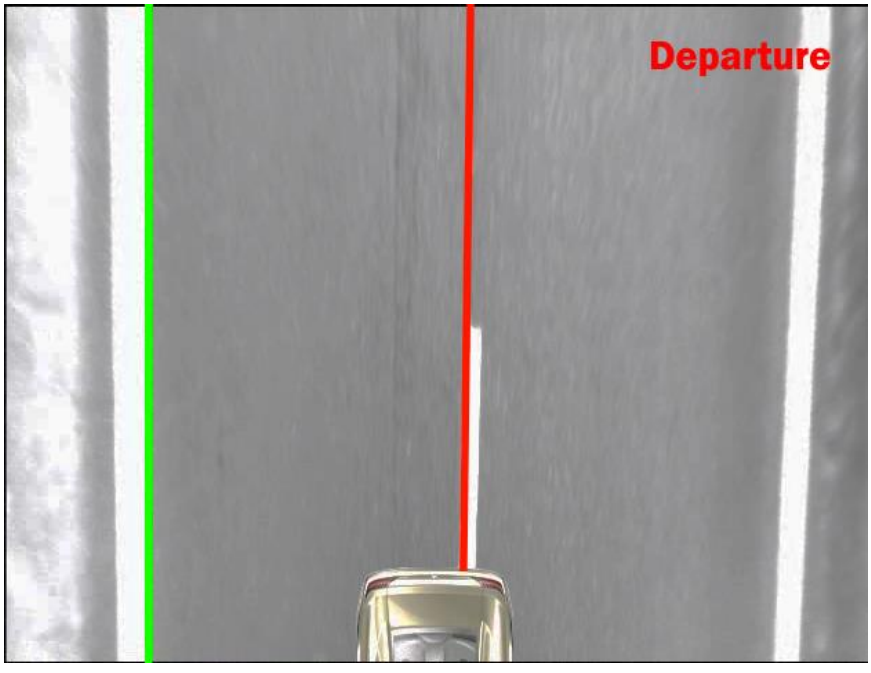

Figure 2: Departure Warning – Screenshot

Typically the LDWS systems are forward looking and use a camera(s) mounted in front of a vehicle. The logiLMD IP core works with the Rear Looking Lane Departure Warning system that offers many advantages: work with a camera mounted at the back end of the vehicle, simpler, robust and fast to compute lane model. The back end mounted cameras are typically used for Rear-View Camera application, Surround View, etc., which means that the Rear Looking LDWS can be added in the FPGA based automotive system with no additional costs in regard to vision sensors.

Functional Description

The Figure 1 presents internal logiLMD architecture. The logiLMD functional blocks are: RGB2Grey, Filt5x17, Sobel3x3, RoiSel, Thinning, AutoCutoff, LMPS, Hough, Selector and DrawLines. The AXI-Stream master interface outputs the video showing the results of the processing stages and is used just for configuration and demonstration purposes. It can be removed as well as the Selector and DrawLines blocks to save FPGA resources.

Color2Grey

It converts the input video stream from RGB888 or YUV4xx format to the only luminance channel Y.

Filt5x17

It convolves the input image with a 5x17 Gaussian kernel. The filtering is used to reduce the Gaussian noise and to attenuate the artifacts.

Sobel3x3

The Sobel3x3 block computes horizontal and vertical gradients by convolving the input image with Sobel kernels.

RoiSel

It selects those pixels within a user defined region of interest.

Thinning

It computes the edge map from the image gradients. In particular it looks for edge points in correspondence of vertical lines.

AutoCutOff

It computes the automatic optimal global threshold discriminating between edge and not edge points to use in the Thinning block.

LMPS

It selects the edge points corresponding to the internal borders of the lane markings. The block acts as a filter preserving only those points corresponding to patterns characterizing the lane marking points.

Hough

It extracts a set of straight lines from the binary map output of the LMPS block. It applies an adaptation of the Hough Transform algorithm for straight lines, a robust fitting technique based on two stages:

- a voting stage, where each edge point votes for a sheaf of straight lines passing through this point. Voting means incrementing a table of accumulators (Hough Table) in the line parameters space. Straight lines are represented in polar coordinates ρ and θ.
- a peak detection stage, where the Hough Table is analyzed to find the local maximum whose (ρ,θ) corresponds to the most voted lines.

Selector

The Selector block is a mux that outputs different video streams, according to a selection register. These video streams are the output of different blocks: RGB2Grey, Gaussian filtering, Thinning, LMPS.

DrawLines

This block overlays straight lines on the output video stream. It can be used to draw the results from the Hough block.

LMD registers

The logiLMD's register interface can be configured as AXI4-Lite compatible interface

Core I/O Signals

Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk	Input	input processing clock
AXI4-Stream signals (slave bus)		
s_axis_tdata (23:0)	Input	Video Data: • for 24-bit RGB input (RED [23:16] ; GREEN [15:8] ; BLUE [7:0]) • for 24-bit YUV444 input (V[23:16] ; U[15:8] ; Y[7:0])) • for 16-bit YUV422 input type only 15:0 is in use (U/V [15:8] ;Y [7:0])
s_axis_tvalid	Input	Valid
s_axis_tuser	Input	Start Of Frame
s_axis_tlast	Input	End Of Line
s_axis_tready	Output	Ready
AXI4-Stream signals (master bus)		
m_axis_tdata (23:0)	Output	Video Data: • for 24-bit RGB input (RED [23:16] ; GREEN [15:8] ; BLUE [7:0]) • for 24-bit YUV444 input (V[23:16] ; U[15:8] ; Y[7:0])) • for 16-bit YUV422 input type only 15:0 is in use (U/V [15:8] ;Y [7:0])
m_axis_tvalid	Output	Valid
m_axis_tuser	Output	Start Of Frame
m_axis_tlast	Output	End Of Line
m_axis_tready	Input	Ready
Register Interface		
AXI4-Lite Interface	BUS	Refer to AMBA AXI version 4 specification from ARM
Auxiliary Signals		
rgb_present	Output	External video present

Embedded Software

The logiLMD outputs a list of straight lines, corresponding to lane markings on the roadway. A higher level reasoning is necessary in order to detect the actual lane, i.e. the one the vehicle is on, to track it and raise a warning when the vehicle departs from it. This high level decision-making process is provided as open source software library.

Verification Methods

The logiLMD is fully supported by Xilinx Vivado design tool. This tight integration tremendously shortens IP integration and verification. A full logiLMD implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Xilinx System Generator for DSP (MathWorks Matlab/Simulink) to source model access

Available Support Products

The logiLMD IP core can be evaluated on the logiADAK Advanced Driver Assistance (ADAS) Development Kits that allow customers to fully evaluate performance on their vehicle or in the laboratory.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.01a	19.11.2012	Initial datasheet release
2.0.1	21.11.2014	Vivado release
2.1.1	26.05.2017	Vivado 2016.4 and support for UltraScale+
2.1.2	10.04.2019	Updates for Vivado 2018.2

The logiLMD core is sourced from Technology Partner
eVS embedded Vision Systems Srl.