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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	XDC
Verification	Reference design simulation
Reference Designs & Application Notes	Please contact Xylon.
Additional Items	
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim®	
Support	
Support provided by Xylon	

Features

- Supports DDR3 SDRAM memory devices on AMD-Xilinx 7 Series FPGAs and Zynq SoC*
- Size-optimized – ideal for low-cost 7 Series FPGAs (Artix-7, Spartan-7)
- 800 Mb/s max bandwidth on Artix-7/Spartan-7 devices (-1, -1L, -1LI speed grades)
- x8/x16 DDR3 SDRAM component data width support
- x8/x16/x32 DDR3 interface data width support
- ARM® AMBA®AXI4 Slave Interface on system side (fabric)
- 8:1 system data width to DDR3 data width ratio
- 4:1 memory to FPGA system interface clock ratio
- Supports single-beat and burst transaction on the AXI4 interface bus
- AXI4 interface INCR and WRAP burst types support
- Programmable burst length on AXI4 interface (16, 32, 64, 128, 256)
- Programmed burst length applies on both read and write memory cycles
- Programmable CAS latency (supported CL5, CL6)

** Currently compatible with HR IO banks only*

Table 1: Example Implementation Statistics for AMD-Xilinx FPGAs

Family (Device)	Fmax (MHz)		DDR3 Width[4]	LUT	FF	IOB[1]	BRAM Tile	OUT_FIFO	IN_FIFO	PLL/ MMCM	BUFG	Design Tools
	AXI4 clk	DDR3 clk										
Artix®-7 (XA7A50T-1)	100	400	8	876	578	38	0	4	1	1	5	Vivado 2021.2
Artix®-7 (XC7A100T-1)	100	400	16	1279	920	48	0	5	2	1	5	Vivado 2021.2
Artix®-7 (XC7A200T-2)	100	400	32	2111	1594	71	0	7	4	1	5	Vivado 2021.2
Spartan®-7 (XC7S50-1)	100	400	16	1269	910	48	0	5	2	1	5	Vivado 2021.2

1) Assuming only DDR SDRAM device signals are routed off-chip
2) Implementation statistics given for Artix-7 and Spartan-7 FPGAs are also valid for the corresponding SoC families
3) Implementation statistics with *C_BURST_WIDTH = 4* and *C_MEM_SAMPLE_CLK_MAN = 1*
4) Please note that the table shows implementation statistics for several SDRAM interface data widths

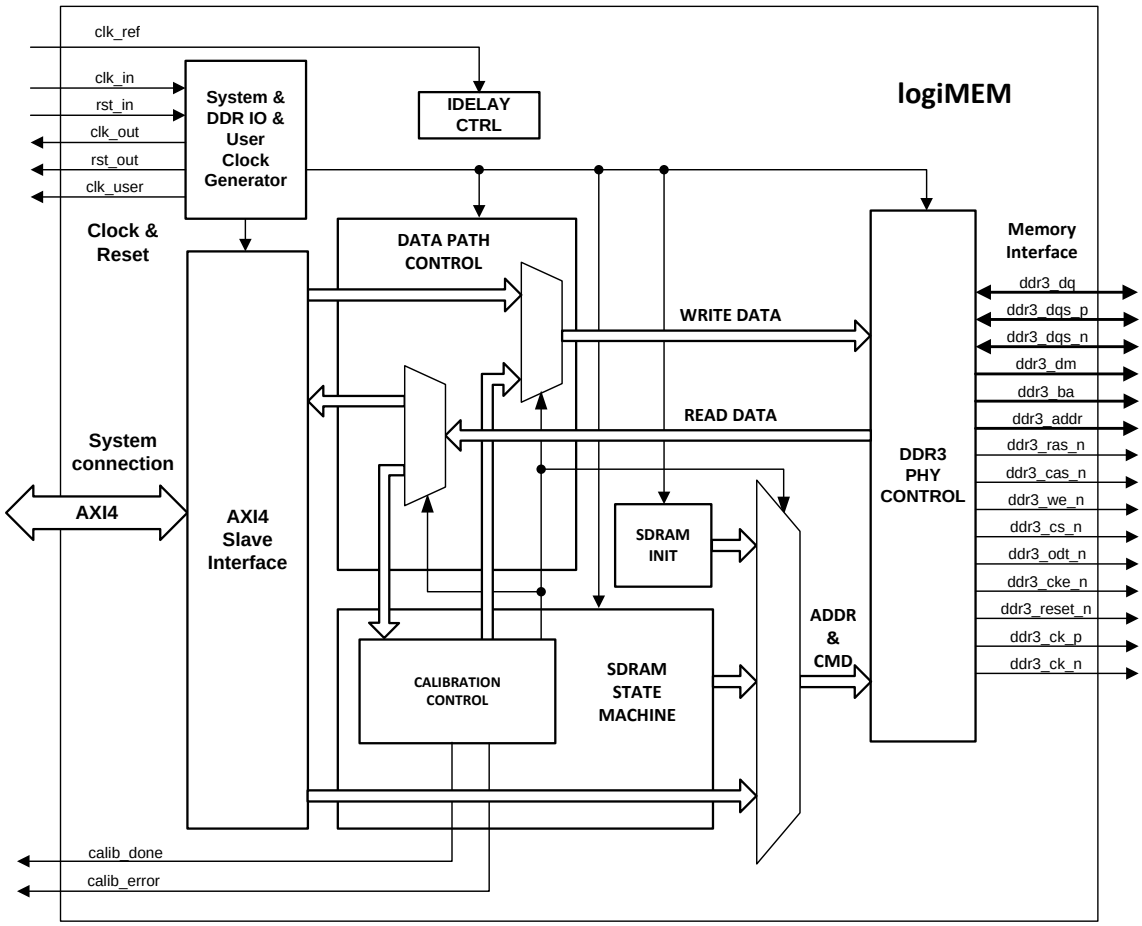

Figure 1: logiMEM Block Diagram

Features (cont)

- Byte Enable signals for masking data supported for write operations (AXI4 interface)
- Configurable DDR3 SDRAM row and column address width
- Configurable DDR3 SDRAM timings
- Supported JEDEC-compliant DDR3 initialization
- Supported memory refresh cycles
- Programmable DDR SDRAM RTT and ODS settings
- DDR3 (1.5 V) and DDR3L (1.35 V) support
- 8-bank support
- 8-word burst support
- On-die termination (ODT) support
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Prepared for AMD-Xilinx Vivado® Design Suite implementation tools
- Simple Plug'n'Play with other logicBRICKS by Xylon® IP cores, such as:
  - logiCVC-ML Compact Multilayer Video Controller
  - logiWIN Versatile Video Controller
  - logiISP Image Signal Processing (ISP) Pipeline

Memory bandwidth

Table 2: Max DDR3 memory bandwidth on Artix-7 and Spartan-7 FPGAs

Artix-7, Spartan-7	Max DDR3 bandwidth (Mb/s)		
Interface	-1L (Vccint= 1.0V)	-1I (Vccint= 0.95V)	-1 (Vccint= 1.0V)
DDR3	800	800	800
DDR3L	800	800	800

Applications

- Video systems and image processing
- Embedded computing
- Communication and Networking equipment
- High performance peripheral equipment

General Description

The logiMEM DDR3 SDRAM Memory Controller is a size-optimized, flexible, parametric and synthesizable Synchronous DRAM Controller that supports industry standard Double Data Rate 3 (DDR3) SDRAM memories on AMD-Xilinx 7 Series FPGAs/SoCs. Its system interface is compliant to ARM's AMBA Advanced eXtensible Interface (AXI4) bus protocol.

"Easy-to-use" parameters and the synthesis for different requirements, optimized for area and speed, auto-routed design makes this IP Core especially suitable for AMD-Xilinx 7 Series FPGA/SoC designs featuring AXI4 bus architecture. It enables an easy connection of processor cores, as well as various peripheral cores, to DDR3 memory chips via AXI4 slave system interface port.

The logiMEM IP Core is fully embedded into the AMD-Xilinx Vivado toolset, and its parametrizable VHDL design allows tuning of slice consumption and features set through an easy-to-use GUI interface. The logiMEM can be smoothly integrated with other logicBRICKS^{TM} IP cores for building of advanced GUI embedded systems.

Functional Description

The logiMEM DDR3 SDRAM memory controller is partitioned into modules as shown in **Figure 1: logiMEM Block Diagram** and described bellow.

Clock generator

This block utilizes PLL/MMCM to generate all the clock signals needed by the memory controller. From the supplied input clock it generates a user interface clock (AXI4 slave clock) or a system clock, all internal clocks, a DDR3 IO clock and freely usable user clocks.

AXI4 Slave Interface (User interface)

The AXI4 slave interface provides an industry-standard bus protocol interface to the memory controller.

The AXI4 slave interface presents a user interface as an AXI4 memory-mapped compliant slave ideal for connecting to processor subsystems. Currently the logiMEM's AXI4 Slave interface enables 64/128/256-bit wide bus connections in accordance with the AXI4 bus specifications. AXI4 data is always 8x wider than the DDR3 memory data bus.

SDRAM INIT

SDRAM INIT block performs a required JEDEC-compliant power-on DDR3 initialization sequence after deassertion of the system reset. After thr DDR3 initialization is complete, the controller can begin issuing commands to the memory, all according to the JEDEC standard.

Calibration Control

Calibration logic performs a timing training of the read datapath to account for system static and dynamic delays. The logiMEM IP core indicates the completed calibration so the internal logic can begin issuing commands to the memory.

SDRAM State Machine

The SDRAM State Machine accepts write/read commands issued by the User interface (AXI4 slave interface) and generates proper commands for memory devices. It also controls memory banks/rows opening and closing, as well as generating memory refresh cycles. It handles all memory device signal sequencing and timing.

Data Path Control

The Data Path Control block routes write data from the User interface block to the PHY Control block and read data from the PHY Control block to the User interface block. It also makes an appropriate format conversion from the User interface data format to the PHY Control block format and vice versa.

PHY control

The PHY control block implements a physical layer for interfacing DDR3 memory devices. It transforms the controller's internal command/address/data signals to a physical layer format required by the DDR3 during command/write accesses and vice versa during read accesses.

Core Modifications

The core is supplied in an encrypted VHDL format, and many logiMEM parameters are configurable prior to the VHDL synthesis. There are many different user-settable parameters defining the required system/DDR3 clock settings, DDR3 memory parameters, advanced settings etc.

In spite of the IP core's great flexibility, there may be instances where source code modification is necessary. If you wish to reach the optimal use of the logiBITBLT core, or to supplement some of your specific functions, you can allow us to tailor the logiMEM to your requirements.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk_ref	Input	200MHz Reference Clock for IOB TAP Delay (IDELAY CTRL).
clk_in	Input	logiMEM's main input clock. Supplied directly to MMCM.
rst_in	Input	Asynchronous system reset. Resets everything: user interface, MMCM, state machine, PHY …).
rst_logic	Input	Asynchronous logic reset (internally synchronized). Resets everything but the MMCM.
rst_out	Output	Output reset, synchronous to output clock (system clock).

Signal	Signal Direction	Description
clk_out	Output	Output clock (buffered) used for AXI4 interface (system clock).
clk_out_nobuf	Output	Unbuffered version of clk_out.
clk_user	Output	Finely adjustable user clock output (buffered).
clk_user_nobuf	Output	Unbuffered version of clk_user.
clk_user2	Output	Coarsely adjustable user clock output 2 (buffered).
clk_user2_nobuf	Output	Unbuffered version of clk_user2.
clk_x2	Output	2x system clock, synchronous to system clock, buffered
clk_x2_nobuf	Output	Unbuffered version of clk_x2
clk_x4	Output	4x system clock, synchronous to system clock, buffered
clk_x4_nobuf	Output	Unbuffered version of clk_x2
clk_x4_90	Output	clk_4x phase shifted by 90°, buffered
clk_x4_90_nobuf	Output	Unbuffered version of clk_x4_90
System Interface		
AXI4 Slave Interface	Bus	AXI4 interface. For more information refer to AMBA AXI specification.
DDR3 SDRAM Signals		
m_clk_p	Output	DDR3 SDRAM clock
m_clk_n	Output	DDR3 SDRAM clock – inverted
m_cke	Output	DDR3 SDRAM clock enable
m_reset_n	Output	DDR3 SDRAM reset
m_cs_n	Output	DDR3 SDRAM chip select
m_ras_n	Output	DDR3 SDRAM command RAS
m_cas_n	Output	DDR3 SDRAM command CAS
m_we_n	Output	DDR3 SDRAM command WE
m_odt	Output	DDR3 SDRAM ODT
m_dm[C_DDR_DATA_WIDTH/8-1:0]	Output	DDR3 SDRAM data mask
m_ba[C_DDR_BADDR_WIDTH-1:0]	Output	DDR3 SDRAM bank address
m_a[C_DDR_ADDR_WIDTH-1:0]	Output	DDR3 SDRAM Row/Column address
m_dq[C_DDR_DATA_WIDTH-1:0]	InOut	DDR3 SDRAM data bus
m_dqs_p[C_DDR_DATA_WIDTH/8-1:0]	InOut	DDR3 SDRAM data strobe
m_dqs_n[C_DDR_DATA_WIDTH/8-1:0]	InOut	DDR3 SDRAM data strobe - inverted
Other Signals		
calib_done	Output	Calibration done (used internally, brought out for user reference)
calib_error	Output	Calibration error (used internally, brought out for user reference)
debug_in	Input	Advanced port; ignore.
debug	Output	Advanced port; ignore.

Verification Methods

The logiMEM is fully supported by the AMD-Xilinx Vivado Design Suite 2021.2 and newer versions. This tight integration tremendously shortens IP integration and verification. A full logiMEM implementation does not require any particular skills beyond general AMD-Xilinx tools knowledge. The encrypted IP supports running simulations in popular simulation tools.

The logiMEM evaluation IP core can be downloaded from Xylon's website and fully evaluated in hardware.

URL: http://www.logicbricks.com/Products/logiMEM.aspx

Recommended Design Experience

The user should have experience in the following areas:

- AMD-Xilinx design tools
- ModelSim

Available Support Products

Xylon provides several free pre-verified reference designs for the most popular AMD-Xilinx evaluation kits. Comprehensive design deliverables include: evaluation logicBRICKS IP cores, hardware design files prepared for AMD-Xilinx Vivado Design Suite, complete Linux OS image, Xylon logicBRICKS software drivers for Linux OS and demo software applications.

To learn more about Xylon's reference designs, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Ordering Information

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Related Information

AMD-Xilinx Programmable Logic

For information on AMD-Xilinx programmable logic or development system software, contact your local AMD-Xilinx sales office, or:

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Revision History

Version	Date	Note
1.1	22.04.2022.	Initial Xylon release.