Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	Reference design simulation
Reference Designs & Application Notes	XPS reference design
Additional Items	logiCRAFT6 evaluation board logiTAP evaluation platform
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports SDR, DDR and DDR2 SDRAM memory types
- 16/32-bit DDR SDRAM data interface (not supported on Spartan-6 devices)
- 8/16/32-bit DDR2 SDRAM data interface (supported only on Spartan-6 devices)
- 32/64-bit SDR SDRAM data interface
- 32/64-bit CoreConnect™ PLBv46 slave system data interface
- Optionally, and in a combination with the logiFLASH Memory controller, supports shared Flash/SDRAM pins
- CoreConnect™ OPB Slave interface or PLBv46 Slave interface for Microblaze connection
- 4 Xilinx CacheLink (XCL) ports for connection of the MicroBlaze cache interface
- 10 Xylon Memory Interface (XMB) ports for connection of various logicBRICKS™ IP cores
- Supports single-beat and burst transaction on the PLB bus
- Supports target-word first cache-line transactions on the PLB bus
- Programmable burst length
- The burst length is valid for both, read and write memory cycles

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	clk	opb_clk									
Spartan®-3E (XC3S1200E-5)	171	235	857	381 (352 / 408)	57	0	0	0	0	N/A	ISE® 11.5
Spartan®-6 (XC6SLX25-3)	212	362	1318	206 (352 / 327)	57	0	0	0	0	N/A	ISE® 11.5
Virtex®-5 (XC5VLX30-3)	372	592	1478	231 (350 / 330)	57	0	0	0	0	N/A	ISE® 11.5

Notes:
1) Assuming 32-bit SDRAM configuration, OPB bus and one XMB interface, "Always close" bank policy.
2) Assuming only SDRAM device signals are routed off-chip

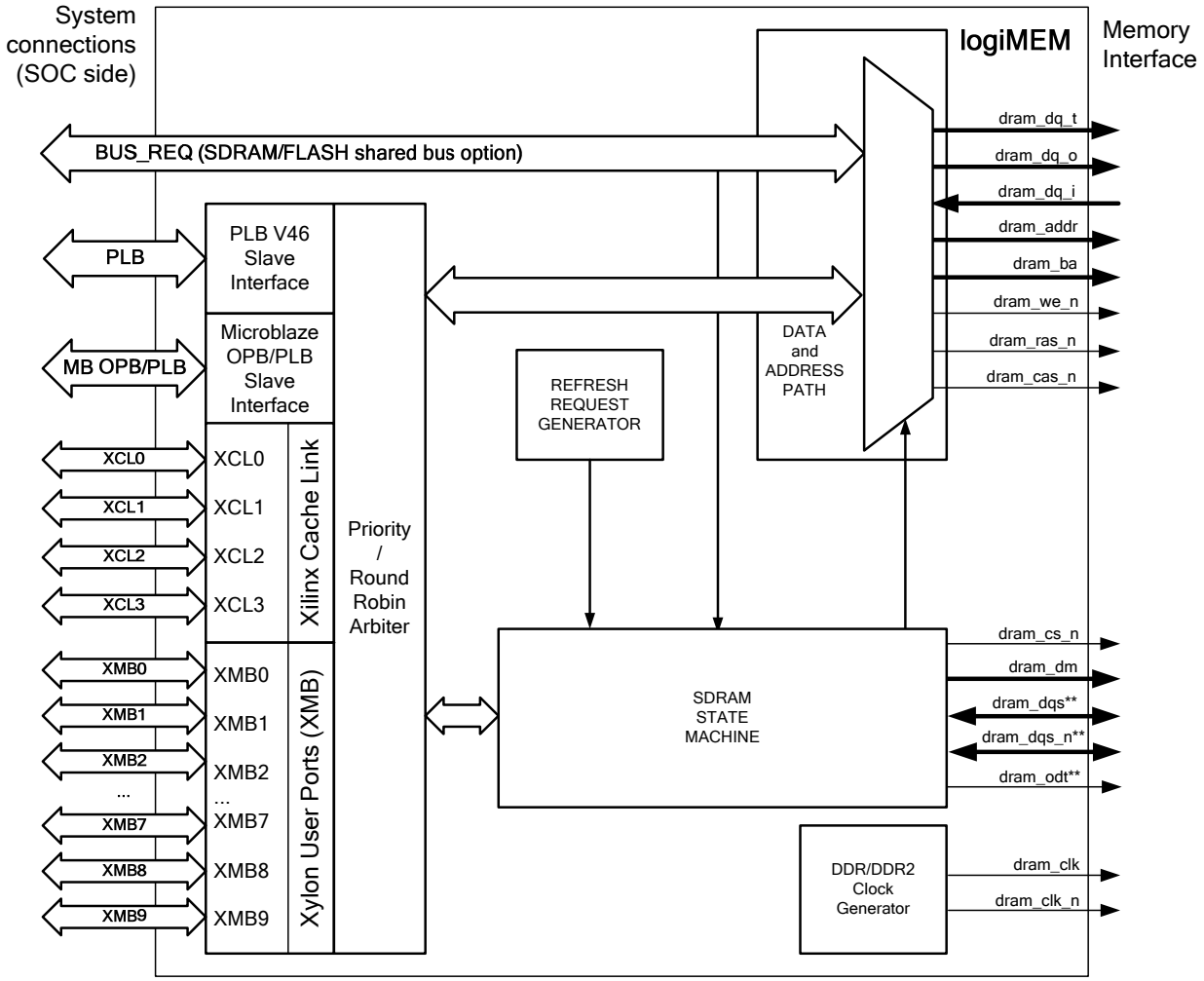

Figure 1: logiMEM Block Diagram

Features (cont)

- Multiple concurrent memory bank access (multi-bank open policy)
- Byte Enable signals for masking data supported for write operations(XMB interface)
- Configurable SDR/DDR/DDR2 SDRAM row and column address width
- Configurable SDR/DDR/DDR2 SDRAM timings
- Supported SDR/DDR/DDR2 SDRAM initialization
- Double memory frequency option on SPARTAN 6 devices (data rate up to 533Mbit)
- Little-Endian connections to memory devices
- Supported memory refresh cycles
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Prepared for Xilinx Platform Studio (XPS) and the EDK
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as:
  - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
  - logiBMP Bitmap 2.5D Graphics Accelerator
  - logiCVC-ML Compact Multilayer Video Controller
  - logiWIN Versatile Video Controller

Applications

- Video systems and image processing
- Embedded computing
- Communication and Networking equipment
- High performance peripheral equipment

General Description

The logiMEM is a flexible, parametric and synthesizable Synchronous DRAM Controller that supports industry standard Double Data Rate (DDR and DDR2) and Single Data Rate (SDR) SDRAM memories. Its system interface is compliant to IBM's CoreConnect Processor Local Bus (PLB) V46, IBM's CoreConnect On-Chip Peripheral Bus (OPB), Xilinx CacheLink (XCL) and Xylon memory interface (XMB).

"Easy-to-use" parameters and the synthesis for different requirements, optimized for an area and speed, auto-routed design makes this IP Core especially suitable for FPGA SoC (System on Chip) designs featuring PLB, OPB, XCL and XMB bus architecture. It enables an easy connection of processor cores, as well as various peripheral cores, to SDR/DDR/DDR2 memory chips. The logiMEM system ports can be configured for a simultaneous support of different bus architectures.

The logiMEM is fully embedded into Xilinx Platform Studio and EDK tools, and its parametrizable VHDL design allows tuning of slice consumption and features set through an easy-to-use GUI interface. The logiMEM can be smoothly integrated with other logicBRICKS™ IP cores for building of advanced GUI embedded systems.

Functional Description

The logiMEM SDR/DDR/DDR2 SDRAM memory controller is partitioned into modules as shown in Figure 1 and described bellow.

Slave PLB Interface

The PLB Slave interface module assures bus control and correct logiMEM's attachment to the PLB bus. Currently the logiMEM's PLB Slave interface enables 32/64-bit wide bus connections in accordance to the CoreConnect bus specifications.

Microblaze Slave OPB/PLB Interface

The Microblaze OPB/PLB Slave interface module assures bus control and correct logiMEM's attachment to the OPB/PLB specifically designed for connecting Microblaze™ CPU interfaces. Currently the logiMEM's OPB Slave interface enables 32-bit wide connections and PLB Slave interface enables 32/64-bit wide bus connections in accordance to the CoreConnect bus specifications.

Xilinx XCL Interface

Xilinx CacheLink (XCL) is a high performance solution for external memory accesses of the MicroBlaze™ cache interface. The MicroBlaze CacheLink interface can be connected directly to the logiMEM memory controller, which integrates the required FSL buffers.

Xylon XMB Interface

Xylon Memory Interface (XMB) is a simple, small, fast and efficient proprietary interface solution for connecting various logicBRICKS™ IP cores to an external SDRAM memory by mean of the logiMEM IP core. The XMB interface supports 32/64-bit single and burst read/write accesses.

Priority Arbiter

The Priority Arbiter arbitrates memory access requests from system modules of all supported interface types: PLB, OPB, XCL and XMB. Simultaneous requests from different modules are granted accordingly to pre-programmed priorities. The logiMEM supports Fixed and Round-Robin prioritization algorithms, and each logiMEM input port can be configured for specific prioritization type.

SDRAM State Machine

The SDRAM State Machine accepts commands issued by the Priority Arbiter and generates commands for memory devices. Supported commands are all types of read/write accesses (including burst accesses), memory banks opening and closing controls for faster open row bank accesses, and the SDR/DDR/DDR2 device initialization sequences.

Refresh Request Generator

The Refresh Request Generator automatically controls SDRAM device's requested refresh cycles. It counts pre-programmed number of clock periods (clk), and have precedence over other system accesses to the memory.

Data and Address Path

The Data and Address Path module accepts address and data from/to system modules and converts them into the memory interface's address and data format. The IBM's CoreConnect bus uses bit and byte labeling accordingly to the Big-Endian format, while the majority of SDR/DDR/DDR2 SDRAM chips supports the Little-Endian format. The Data and Address path module takes care on Endianess and makes a proper conversion requested by the Little-Endian memory devices.

Core Modifications

The core is supplied in an encrypted VHDL format and many logiMEM parameters are configurable prior to VHDL synthesis. There are more than 60 different user-settable parameters defining the IP's timings, port configurations, Xilinx device family, etc.

In spite of such a great IP core's flexibility there may be instances where source code modification is necessary. If you wish to reach the optimal use of the logiBITBLT core, or to supplement some of your specific functions, you can allow us to tailor the logiMEM to your requirements.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
refclk	Input	200MHz Reference Clock for IOB TAP Delay. Used only for Virtex4 and Virtex5 devices
rst	Input	Synchronous system reset. Reset all XMB interfaces and internal state machine.
clk	Input	System clock. This clock is used for internal logiMEM operation, PLB and XMB interfaces

Signal	Signal Direction	Description
clk_90	Input	System clock with phase shift of 90 degrees. Used only for DDR SDRAM configuration.
System Interface		
PLB Slave	Bus	PLB interface
OPB Slave	Bus	OPB Interface
MB-PLB Slave	Bus	Microblaze PLB Interface
XCL	Bus	Xilinx Cache Link Interface
Xylon Memory Bus (XMB) Interface		
userN_req	Input	Memory request
userN_wr	Input	Memory write
userN_ack	Output	Memory acknowledge
userN_addr[C_ADDR_WIDTH-1:0]	Input	Memory address for read/write request
userN_data[C_NATIVE_DWIDTH-1:0]	Input	Write data bus
userN_data_be[C_NATIVE_DWIDTH/8-1:0]	Input	Write enable individual bytes during data write
userN_wrack	Output	Memory data acknowledge for write cycle
userN_burst_len[C_USER_BURST_WIDTH-1:0]	Input	Burst length bus
userN_data_out[C_NATIVE_DWIDTH-1:0]	Output	Read data bus
userN_data_valid	Output	Data valid signal during data read
SDRAM Signals		
dram_clk[C_DRAM_CLK_PAIRS-1:0]	Output	SDRAM clock signal
dram_clk_n[C_DRAM_CLK_PAIRS-1:0]	Output	SDRAM clock signal – inverted
dram_cke	Output	SDRAM clock enable
dram_cs_n	Output	SDRAM chip select signal
dram_ras_n	Output	SDRAM command RAS
dram_cas_n	Output	SDRAM command CAS
dram_we_n	Output	SDRAM command WE
dram_dm[C_DRAM_DATA_WIDTH-1:0]	Output	SDRAM data masks, mask individual bytes during data write
dram_ba[C_DRAM_ADDR_BNK_WIDTH-1:0]	Output	SDRAM bank address
dram_addr[C_DRAM_ADDR_WIDTH-1:0]	Output	Row/Column SDRAM address
dram_dq[C_DRAM_WIDTH-1:0]	InOut	SDRAM data bus
dram_dqs[C_DRAM_DATA_WIDTH/8-1:0]	InOut	DDR/DDR2 SDRAM data strobe
dram_dqs_n[C_DRAM_DATA_WIDTH/8-1:0]	InOut	DDR/DDR2 SDRAM data strobe inverted
dram_odt[C_DRAM_ODT_WIDTH-1:0]	Output	DDR2 SDRAM on-die termination output
SDRAM Signals		
bus_req	Input	SDRAM/FLASH bus request
bus_ack	Output	SDRAM/FLASH bus acknowledge
bus_we_n	Input	SDRAM shared we_n signal
bus_cas_n	Input	SDRAM shared cas_n signal
bus_ras_n	Input	SDRAM shared ras_n signal
bus_addr[C_DRAM_ADDR_WIDTH-1]	Input	SDRAM/FLASH address bus
bus_ba[C_DRAM_ADDR_BNK_WIDTH-1:0]	Input	SDRAM/FLASH bank address bus
bus_data_o[C_DRAM_ADDR_WIDTH-1]	Input	SDRAM/FLASH data bus write
bus_data_t[C_DRAM_ADDR_WIDTH-1]	Input	SDRAM/FLASH data bus three-state control
bus_data_i[C_DRAM_ADDR_WIDTH-1]	Output	SDRAM/FLASH data bus read

Verification Methods

The logiMEM is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiMEM implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on logiCRAFT6 Xylon development platform, which is designed especially for developers working in the fields of multimedia and infotainment. This platform demonstrates modularity on all levels: software, board, FPGA, and IP cores. The platform makes excellent development tool particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
3.00	24.03.2009	Initial Xylon release – new doc template
3.01.a	06.10.2009	3 shared input ports added
3.01.b	22.10.2009	Bug fix for 32-bit PLB data width
3.01.c	11.12.2009	Bug fix related to last added 3 shared input ports
4.00	07.04.2010	Added DDR2 SDRAM support. Added MB PLB interface. Added Spartan 6 support. New doc template.