## Xylon d.o.o.

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## Features

- Adds MOST® (Media Oriented System Transport) connectivity to Xilinx® FPGAs / SoCs
- MediaLB® technology, licensed from SMSC®, enables interconnections with different INICs
- Supports Xilinx Zynq™-7000 All Programmable SoC, Spartan®-6 and 7 Series FPGA families
- Compliant with the MLB Specification Version 4.2
- Supports 3-pin and 6-pin interface to INICs
- Multiple clock speeds supported:
  - 3-pin: 256, 512, 1024xFs
  - 6-pin: 2048, 3072, 4096xFs (depending on device's speed grade)

## Core Facts

| Provided with Core | |
|---|---|
| Documentation | User's Manual |
| Design File Formats | Encrypted VHDL |
| Constraints Files | Reference design ucf |
| Verification | Reference design |
| Reference Designs & Application Notes | XPS reference design |
| Additional Items | logiCRAFT-CC evaluation platform<br>logiCRAFT-CC adapter board for MOST® PHY+ Boards OS81xxx<br>SW drivers |
| **Simulation Tool Used** | |
| ModelTech's Modelsim | |
| **Support** | |
| Support provided by Xylon | |

**Table 1: Example Implementation Statistics for Xilinx® FPGAs and SoCs**

| Family (Device) | Fmax (MHz) | | Config[1] | LCs | Slices (FFs/ LUTs) | IOB[2] | BUFG | BUFR | BRAM | MULT/ DSP48/E | PLL/ CMT | GTx | Design Tools |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | mlb_clk[3] | rclk | | | | | | | | | | | |
| Spartan®-6 (XC6SLX150T-3) | 205 | 185 | 1. | 2304 | 360 (622/691) | 3 | 1 | N/A | 4 | 0 | 0 | 0 | ISE® 14.4 |
| | | | 2. | 2477 | 387 (640/762) | 10 | 2 | N/A | 4 | 0 | 1 | 0 | |
| | | | 3. | 1760 | 275 (538/523) | 10 | 2 | N/A | 2 | 0 | 1 | 0 | |
| Zynq™-7000 (XC7Z020-2) | 205 | 212 | 1. | 2490 | 389 (647/720) | 3 | 0 | 1 | 4 | 0 | 0 | 0 | ISE® 14.4 |
| | | | 2. | 2867 | 448 (650/700) | 10 | 1 | 3 | 4 | 0 | 1 | 0 | |
| | | | 3. | 1984 | 310 (558/489) | 10 | 1 | 3 | 2 | 0 | 1 | 0 | |

Notes:
1) Configurations:
   1. 3-pin, 1024xFs, two channels, 32-bit AXI4-Lite register interface.
   2. 6-pin, 4096xFs, two channels, 32-bit AXI4-Lite register interface.
   3. 6-pin, 4096xFs, two hardcoded control channels, one TX, one RX, 32-bit AXI4-Lite register interface.
2) Assuming only MLB interface signals are routed off-chip, register interfaces are connected internally.
3) Maximum MLB interface clock is defined by specification. The value mentioned is maximum achievable in selected families.

- Scalable data rate for all MOST Network data transport methods:
  - Synchronous
  - Asynchronous
  - Control
  - Isochronous
- Supports up to 63 logical RX and TX channels
- Simple programming of control registers through CoreConnect™ PLBv4.6 or ARM® AMBA® AXI4-Lite interface
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK
- Simple Plug'n'Play with other Xylon logicBRICKS IP cores, such as:
  - logiPCIECTRL PCIe Companion Chip Controller
  - logiMEM Flexible Memory Controller

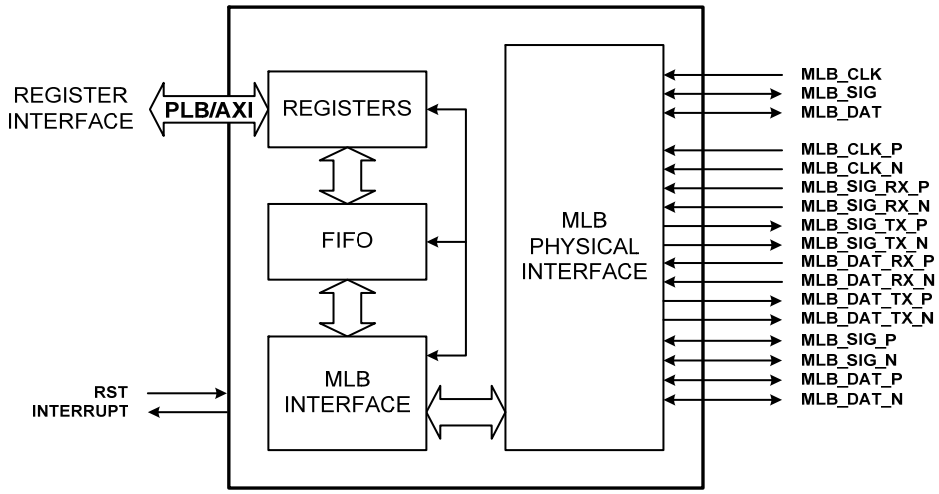


**Figure 1: logiMLB Architecture**

## Applications

Figure 2 and Figure 3 outline two typical logiMLB application scenarios.

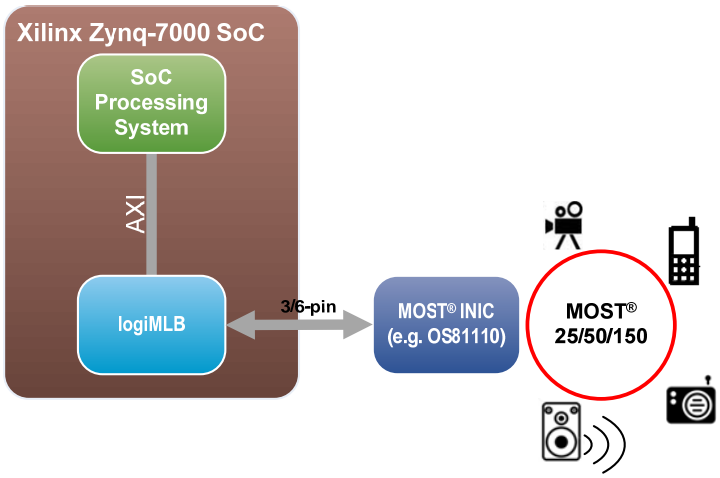


**Figure 2: logiMLB Typical Application 1**

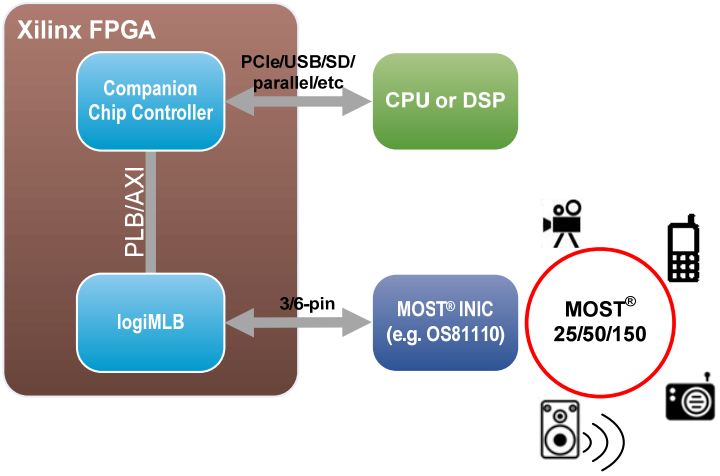


**Figure 3: logiMLB Typical Application 2**

- Car Infotainment and Telematics
- AutoPCs

## General Description

The logiMLB IP core from Xylon's logicBRICKS IP library supports implementation of the SMSC's Media Local Bus (MediaLB) inter-chip communication technology in Xilinx FPGA and an efficient transport of multimedia data through SMSC's intelligent network interface controllers (INICs) onto a Media Oriented System Transport (MOST) network. The MOST networks are infotainment backbones in many cars and de facto industry standard for automotive multimedia networking of high-bandwidth audio, video and control information or network data.

The logiMLB Media Local Bus Interface IP Core complies with the latest MLB Specification version 4.2, and works with all MOST network generations – MOST25/MOST50/MOST150. It supports a 3-pin single-ended MediaLB connection with up to 1024Fs, and a 6-pin differential connection with up to 4096Fs. The logiMLB provides internal buffering and support for up to 63 TX and RX channels.

Support for a new packet channel, which is compatible with Ethernet, enables the integration of Internet-based services with multimedia systems within the car. The emerging multimedia systems based on FPGA technology provide an unmatched flexibility, i.e. use of multiple logiMLB instances within a single Xilinx FPGA/SoC chip can support various network topologies (ring, daisy-chain and star), easy interfacing with standard embedded processors or bridging between different networks.

The logiMLB IP core's deliverables include encrypted VHDL source files prepared for Xilinx Platform Studio (XPS) and the EDK, and IP core's device drivers for interfacing with the MOST NetServices Application Programming Interface (API).

## Functional Description

The logiMLB Media Local Bus IP core's internal structure is shown on the block diagram on Figure 1.

The most important functional blocks are MLB interface block, MLB physical interface block, FIFOs and Registers.

### MLB Interface Block

The MLB Interface Block is a major part of the logiMLB IP core. It handles the MLB specified data link layer and takes care of the proper channel addressing, command receiving/sending, error handling and data transfer. Separated receive and transmit state machines handle receive and transmit protocol for each logical channel.

The MLB Interface Block supports all MediaLB data transfer methods: Control, Asynchronous, Synchronous and Isochronous.

### MLB Physical Interface

The MLB Physical Interface Block consists of input/output sampling logic and clock generation. Depending on MLB interface, 3 or 6-pin, different IO standard and sampling mechanisms are used. Additionally in 6-pin mode, a PLL with internal feedback is used to generate required clocks according to 1:1 or 2:1 clock modes.

### FIFOs

The IP core provides one RX/TX FIFO, which is used for temporary data storage, per each MLB logical channel. The FIFOs optimize usage of MLB bandwidth and resynchronize incoming/outgoing data between the MLB clock and on-chip system clock.

Each FIFO is capable of storing 2kB of data, which limits the MLB control and asynchronous packet size to 2048 bytes, more than the maximum packet size defined by Port Message Protocol, 1526 bytes.

### Registers

The CPU can access all registers either through the CoreConnect PLBv4.6 or through the ARM AMBA AXI4-Lite buses. The registers are separated in the general logiMLB and channel registers groups.

## Core Modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. The following logiMLB configuration parameters are selectable prior to VHDL synthesis:

**Table 2: logiMLB VHDL configuration parameters**

| Parameter | Description |
|---|---|
| C_REGS_INTERFACE | Register interface type: PLBv46 or AXI4-Lite |
| C_REGS_LITTLE_ENDIAN | logiMLB register interface Endianess |
| C_MLB_INTERFACE | MLB pin interface: 3 or 6-pin |
| C_MLB_DEVICE_ADDR | MLB device address |
| C_MLB_SPEED | MLB clock speed: 256,512,1024,2048,3072,4096xFs |
| C_NUM_OF_CHANNELS | Number of logical channels: 1-63 |
| C_BUFF_ALMOST_EMPTY | Buffer almost empty flag: 1-510 |
| C_BUFF_ALMOST_FULL | Buffer almost full flag: 1-510 |
| C_DIFF_HALF_BANK | Data and signal pins on different FPGA half banks |
| C_IO_BANK_USED | FPGA bank in which MLB pins are placed |
| C_IN_CLK_PHASE | Input sampling clock phase offset in relation to MLB clock |
| C_OUT_CLK_PHASE | Output sampling clock phase offset in relation to MLB clock |
| C_CH_HARD_CODE | Configure channel type, direction and address with generic parameters instead of registers |
| C_CH_TYPE | Channel type. 0 = synchronous, 1 = asynchronous, 2 = control, 3 = isochronous. |
| C_CH_DIR | Channel direction. 0 = RX, 1 = TX. |
| C_CH_ADDR | Channel address. Range 2 to 126 but only even addresses supported |

The logiMLB has been constructed with regard to adaptability to various use cases and systems. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach the optimal use of the logiMLB core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiMLB to your requirements. The logiMLB source code (VHDL sources) is available at additional cost from Xylon.

## Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

**Table 3: Core I/O Signals**

| Signal | Signal Direction | Description |
|---|---|---|
| **Global Signals** | | |
| RST | Input | Global synchronous reset |
| INTERRUPT | Output | logiMLB Interrupt signal, level sensitive, high active |
| **Register Interface** | | |
| PLBV46 Slave Interface | Bus | Refer to Xilinx-IBM Core connect specification |
| AXI4-Lite Interface | Bus | Refer to AMBA AXI version 4 specification from ARM |
| **MLB Interface Signals** | | |
| MLB_CLK | Input | MLB 3-pin interface clock |
| MLB_SIG | Input/Output | MLB 3-pin interface signal |
| MLB_DAT | Input/Output | MLB 3-pin interface data |
| MLB_CLK_P | Input | MLB 6-pin interface clock, positive |
| MLB_CLK_N | Input | MLB 6-pin interface clock, negative |
| MLB_SIG_RX_P [1)] | Input | MLB 6-pin interface signal input, positive |
| MLB_SIG_RX_N [1)] | Input | MLB 6-pin interface signal input, negative |
| MLB_SIG_TX_P [1)] | Output | MLB 6-pin interface signal output, positive |
| MLB_SIG_TX_N [1)] | Output | MLB 6-pin interface signal output, negative |
| MLB_DAT_RX_P [1)] | Input | MLB 6-pin interface data input, positive |
| MLB_DAT_RX_N [1)] | Input | MLB 6-pin interface data input, negative) |
| MLB_DAT_TX_P [1)] | Output | MLB 6-pin interface data output, positive |
| MLB_DAT_TX_N [1)] | Output | MLB 6-pin interface data output, negative |
| MLB_SIG_P [2)] | Input/Output | MLB 6-pin interface signal, positive |
| MLB_SIG_N [2)] | Input/Output | MLB 6-pin interface signal, negative |
| MLB_DAT_P [2)] | Input/Output | MLB 6-pin interface data, positive |
| MLB_DAT_N [2)] | Input/Output | MLB 6-pin interface data, negative |

Notes:
1) Implementation in Spartan-6 FPGA family
2) Implementation in Xilinx Zynq-7000 All Programmable SoC and 7 Series FPGA families

## Verification Methods

The logiMLB is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiMLB implementation does not require any particular skills beyond general Xilinx tools knowledge. The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim. The logiMLB is verified in simulation using SMSC INIC bus functional model while extensive hardware testing was performed with SMSC MediaLB Interface Test Bench v2.1.

## Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

## Available Support Products

Xylon logicBRICKS IP cores can be evaluated on Xylon's logiCRAFT-CC Companion Chip development platform, which is designed especially for developers working in the fields of multimedia and infotainment. The platform demonstrates modularity on all levels: software, board, FPGA, and IP cores. The logiCRAFT-CC platform makes an excellent development tool, particularly appropriate for the development of embedded systems with strong graphics capabilities.

The logiCRAFT-CC Companion Chip Platform:

URL: http://www.logicbricks.com/Products/logiCRAFT-CC.aspx

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

## Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
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San Jose, CA 95124
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Fax: +1 408-559-7114
URL: www.xilinx.com

### SMSC

SMSC is a leading provider of silicon solutions for the MOST automotive networking.

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Hauppauge, New York 11788
Phone: +1 631-435-6000
URL: www.smsc.com

### MOST Cooperation

The MOST Cooperation was founded in 1998 to standardize MOST Technology as a global standard for multimedia networking.

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URL: www.mostcooperation.com

## Revision History

| Version | Date | Note |
|---|---|---|
| 1.00 | 13.09.2011. | Initial release |
| 1.01 | 23.11.2011. | 6-pin support, channel hardcode support |
| 1.02 | 21.01.2013. | Added support for Xilinx® Zynq™-7000 All Programmable SoC and 7 Series FPGA families |