Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Reference Designs & Application Notes	Xilinx Vivado® IP Integrator reference design
Additional Items	SW drivers, API and post-processing library
Simulation Tool Used	
Vivado Simulator	
Support	
Support provided by Xylon	

Features

- Advanced HOG/SVM object classification core for support of Pedestrian Detection in camera-based video systems
- Supports Xilinx® Zynq®-7000 AP SoC
- Supports resolutions up to 1024x1024
- Support for multiple scale detection
- Run-time variable image size
- ARM® AMBA® AXI4 compliant Memory Mapped Register Interface
- AXI4 Slave Stream Video Input Interface
- Support RGB(8:8:8) and YUV(4:2:2) video stream format
- High Input Data rate (> 120 Mpixels per Second)
- High Throughput (> 7.6 GMAC/sec for the classification stage)
- Low Latency (< 8 lines)
- Advanced HOG/SVM based algorithms
- Classifier trained on wide range of automotive scenarios
- Run-time loadable classifier
- Vivado reference design including demo software application
- C code API and post-processing library available

Applications

- Driving Assistance Systems
- Video Surveillance
- Robot Navigation
- Assistive Technology for the Visually Impaired
- Content Based Indexing
- Advanced Human-Machine Interfaces

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) [1] sysgen_clk	LCs	Slices [2] (FFs/ LUTs)	IOB	CMT	BRAM [3]	DSP48A	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z045-2)	240	~14,230	2,224 (8,141/5,965)	0	0	50	44	0	N/A	Vivado® 2014.2

Notes:

1) The maximum pixel rate is half Fmax
2) Assuming configuration with default IP parameters
3) Number of RAMB18

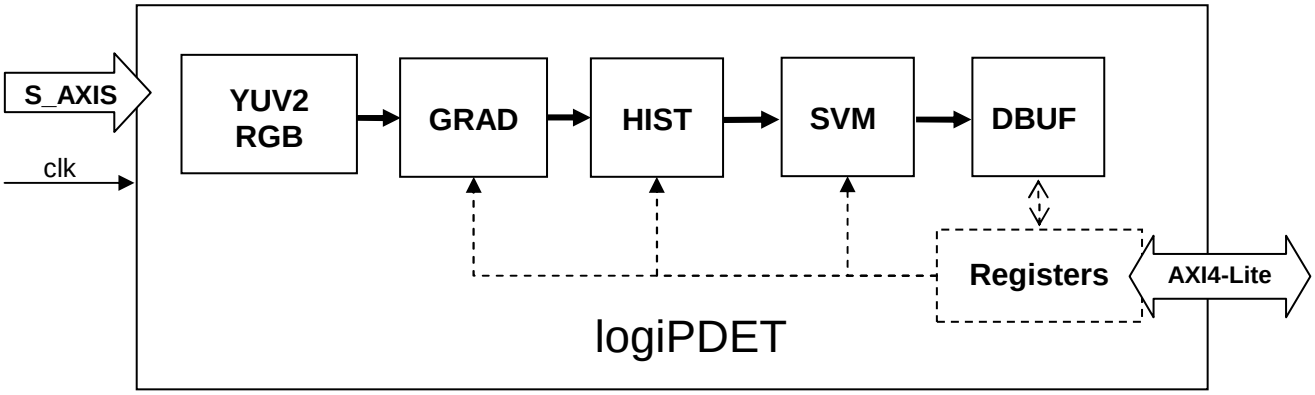

Figure 1 : logiPDET Architecture

General Description

The logiPDET is an HOG/SVM-based pedestrian detection IP core, developed for vision-based embedded applications, from the Xylon logicBRICKS IP core library. The algorithm follows a discriminative approach. It combines a HOG-based descriptor and a SVM classifier.

HOG (Histogram of Oriented Gradients) is a descriptor designed to encode pedestrian structure. SVM (Support Vector Machine) is a non probabilistic binary linear classifier. The core works at a single scale, i.e. the classifier is trained to recognize pedestrian at a fixed size. Extension to multiple scales is given by inserting the core in a framework that provides it with a sequence of re-scaled versions of the same input frame. In this way it is possible to detect pedestrians moving in an arbitrary range of distance.

The core is provided with a built-in pedestrian classifier, but users can load their own classifier via software API at run-time.

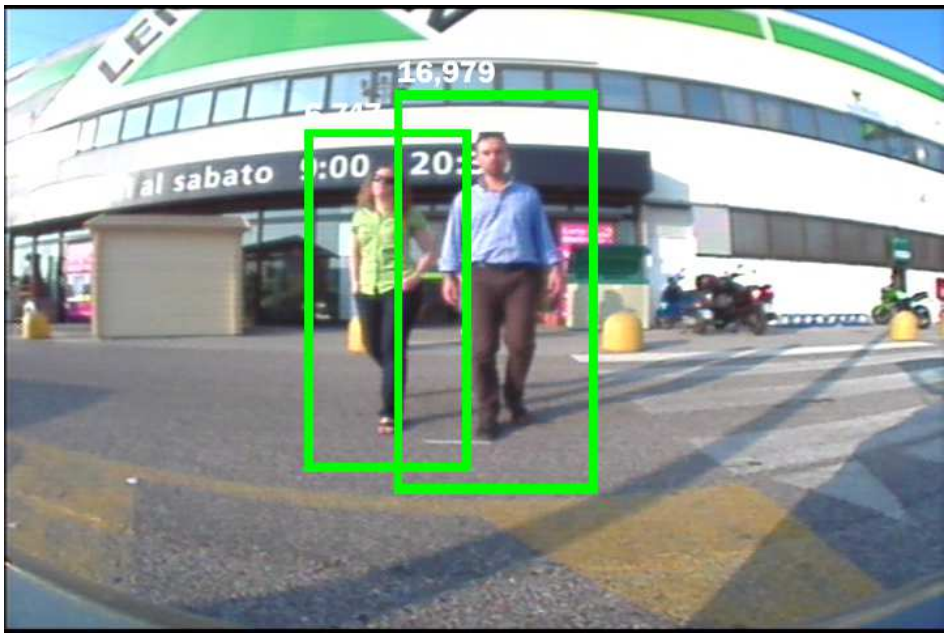

Figure 2: Pedestrian Detection – Screenshot

Functional Description

The Figure 1 presents internal logiPDET IP core's architecture. The logiPDET functional blocks are: YUV2RGB, GRAD block, HIST block, SVM block, DBUF block and PDET Registers.

YUV2RGB

This block is optionally included in case the input video format is 16-bit YUV422. The block converts the video stream from YUV422 to 24-bit RGB888.

GRAD block

The GRAD block computes gradient of the input RGB image. The gradient orientation is quantized into 8 bins in 0°-180°. For each input pixel the GRAD block returns the index of the orientation bin (0..7), the fractional part of the quantization, and the gradient magnitude.

HIST block

The HIST block generates the 8-bins oriented gradient histograms (HOG) for each 8x8 cell of the input image. It returns, in parallel, the bins of the cell histograms corresponding to the current position of the detection sliding window.

SVM block

The SVM block is responsible of the histogram block normalization (a block is composed by 2x2 adjacent cells) and of the estimation of the confidence (score) on the current detection window classification by calculating the inner product between the window descriptor vector and the classifier vector.

DBUF block

The DBUF block queues in the output double buffer the detected pedestrians having a score greater than a user defined threshold. For each of these pedestrians, detected at a certain scale of the sequence, scale, position and score are memorized in the output buffer and a flag is asserted at the end of the computation in order to alert the CPU that the processing results are ready to be read out.

PDET Registers

The PDET register interface can be configured as AXI4-Lite interface.

Core I/O Signals

Descriptions of all signals I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk	Input	input processing clock
AXI4-Stream signals (slave bus)		
s_axis_tdata(23:0)	Input	Video Data: • for 24-bit RGB input (RED [23:16] ; GREEN [15:8] ; BLUE [7:0]) • for 16-bit YUV422 input type only 15:0 is in use (U/V [15:8] ;Y [7:0])
s_axis_tvalid	Input	Valid
s_axis_tuser	Input	Start Of Frame
s_axis_tlast	Input	End Of Line
s_axis_tready	Output	Ready
Register Interface		
AXI4-Lite Interface	BUS	Refer to AMBA AXI version 4 specification from ARM

Verification Methods

The logiPDET IP core is fully supported by Xilinx Vivado design tool. This tight integration tremendously shortens IP integration and verification. A full logiPDET implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Xilinx System Generator for DSP (MathWorks Matlab/Simulink) to source model access

Available Support Products

The logiPDET IP core can be evaluated on the Xilinx Zynq-7000 AP SoC based logiADAK Automotive Driver Assistance Kit. The logiADAK is a great programmable platform for upcoming automotive driver assistance applications that require intensive real-time video processing, parallel execution of multiple advanced algorithms and versatile interfacing with sensors and vehicle's communication backbones.

The logiADAK allows customer to fully evaluate the logiPDET IP core in laboratory or on the test vehicle in real traffic and road conditions.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.01.a	19.11.2012	Initial datasheet release
1.02.a	25.03.2014	Added run-time loadable classifier feature
2.0.1	24.11.2014	Vivado release

The logiPDET core is sourced from Technology Partner eVS embedded Vision Systems Srl.