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Features

- Available under terms of the SignOnce IP License
- Supports Spartan-3/3E/3L, Spartan-II/E, Virtex-II Pro/X, Virtex-II, Virtex-/E, Virtex-4 FPGAs
- Infrared Remote Controller receiver supporting standard Remote controller devices
- NEC and RC-5 protocols supported
- NEC message check by comparing normal and inverted received address and data values can be turned off
- Auto repeat supported
- Receive FIFO for 16 address-command pairs
- Optimized for low slice count
- Parametrizable VHDL design that allows tuning of slice consumption and features set
- CoreConnect™ OPB compliant
- Prepared for Xilinx Platform Studio (XPS) and the EDK

Core Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL, netlists, VHDL RTL sources available at extra cost
Constraint Files	logiRC.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	EDK sample design
Additional Items	Xylon logiCRAFT2 evaluation platform
Simulation Tool Used	
ModelSim	
Support	
Support provided by Xylon	

Application

- Car Infotainment
- Home Entertainment

Table 1: Core Implementation Data (NEC protocol configuration)

Family	Example Device	Fmax (MHz)	Slices	IOBs[1]	GCLK	BRAM	MULT	DCM/DLL	PPC	Design Tools
Spartan-3™	XC3S50-5	117	211	73	1	0	0	0	N/A	ISE 8.1.03i
Spartan-3E™	XC3S100E-5	114	222	73	1	0	0	0	N/A	ISE 8.1.03i
Virtex-4™	XC4VFX12-12	212	231	73	1	0	0	0	0	ISE 8.1.03i
Virtex-II Pro™	XC2VP2-7	187	203	73	1	0	0	0	N/A	ISE 8.1.03i
Spartan-IIE™	XC2S50-7	89	183	72	1	0	0	0	N/A	ISE 8.1.03i

*1 – Assuming all core I/Os are routed off-chip

Table 2: Core Implementation Data (RC5 protocol configuration)

Family	Example Device	Fmax (MHz)	Slices	IOBs[1]	GCLK	BRAM	MULT	DCM/DLL	PPC	Design Tools
Spartan-3™	XC3S50-5	121	162	73	1	0	0	0	N/A	ISE 8.1.03i
Spartan-3E™	XC3S100E-5	121	175	73	1	0	0	0	N/A	ISE 8.1.03i
Virtex-4™	XC4VFX12-12	185	189	73	1	0	0	0	0	ISE 8.1.03i
Virtex-II Pro™	XC2VP2-7	183	166	73	1	0	0	0	N/A	ISE 8.1.03i
Spartan-IIE™	XC2S50-7	120	136	72	1	0	0	0	N/A	ISE 8.1.03i

*1 – Assuming all core I/Os are routed off-chip

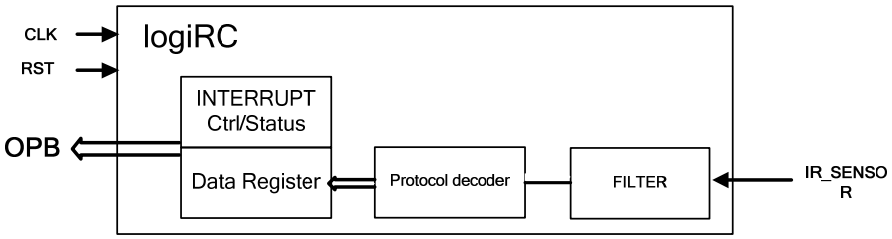

Figure 1: logiRC Block Diagram

General Description

The logiRC core – Remote Controller receiver enables message reception and decoding from standard remote controllers such us TV or DVD controllers. The IP core receives digital messages from a low cost IR (photodiode) receiver connected to a single FPGA pin. An example IR receiver is shown on Figure 2. The logiRC filters and decodes two popular IR remote controller standards: NEC and RC-5. Decoded characters are stored in small internal FIFO, and can be passed to system via the CoreConnect™ OPB bus. The software can control the logiRC through embedded register, while the FIFO status can be checked by polling or by an interrupt. The logiRC is prepared for Xilinx Platform Studio (XPS) and the EDK, and can be smoothly integrated into larger designs. All core's parameters can be easily set through XPS GUI interface.

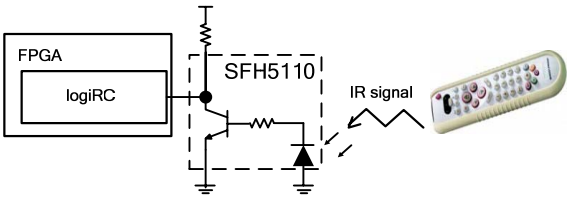

Figure 2 : Infrared Remote Controller featuring logiRC

Functional Description

The logiRC is a small and efficient IP core that consists of few sub modules: input filter, protocol decoder, registers and FIFO sub module.

Input Filter

The input filter passes only properly shaped input RC messages and removes eventual glitches.

Protocol Decoder

The logiRC IP core can be configured for NEC or RC-5 IR RC protocols at the synthesis time. Set up protocol decoder checks filtered messages and extracts address and control code information from them. Wrongly formatted messages are neglected. Correctly received data are stored into an internal FIFO.

Registers and FIFO

The logiRC features only Status and Control registers, and its SW control is very simple. The 16 locations deep FIFO is implemented in distributed CLB RAM due to its small size, and therefore it does not consume the block RAM. The registers are basically used for FIFO and interrupt control

Core parameters

Table 3: Core Parameters

Parameter	Description	Value
NEC_RC5_SELECT	Protocol selection NEC/RC-5	0-NEC 1-RC5
OPB_CLOCK_FREQ	OPB BUS CLOCK	Integer

Pinout

Table 4: Core Signal Pinout

Signal	Type	Description
OPB	inout	OPB CoreConnect™ bus interface
INTERRUPT	out	Interrupt request
RX_DATA_IN	in	Input from the IR sensor, i.e. SFH5110 chip

Verification methods

The logiRC is fully embedded into Xilinx Platform Studio and EDK tools. This tight integration with Xilinx integrated development environment tremendously shortens IP integration and verification time.

The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim.

The simulation and the implementation of the core do not require any particular skills beyond general Xilinx tools knowledge.

Core has been tested in various FPGA implementations, and in combination with various standard IR remote controllers.

Recommended design experience

The users should have experience in the following areas:

- Xilinx ISE tools and the EDK
- ModelSim

Available Support Products

All logicBRICKS™ IP cores can be evaluated, tested and used on Xylon's logiCRAFT2 Multimedia and Infotainment Evaluation/Development platform.
The logiCRAFT2 is Spartan-3TM centric platform capable of driving up to three displays. The platform can simultaneously display different video streams on each screen.
Besides unique display driving capabilities, the logiCRAFT2 supports many networking types. The logiCRAFT2 is expandable and enables rapid hardware prototyping.

Detailed logiCRAFT2 info can be found at **http://www.logicbricks.com/html/evaluation_boards.htm.**

Ordering Information

When inquiring please introduce following inquiring/order codes.

logiRCeconf	Encrypted VHDL source
logiRCvhdl	VHDL source code

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Related Information

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