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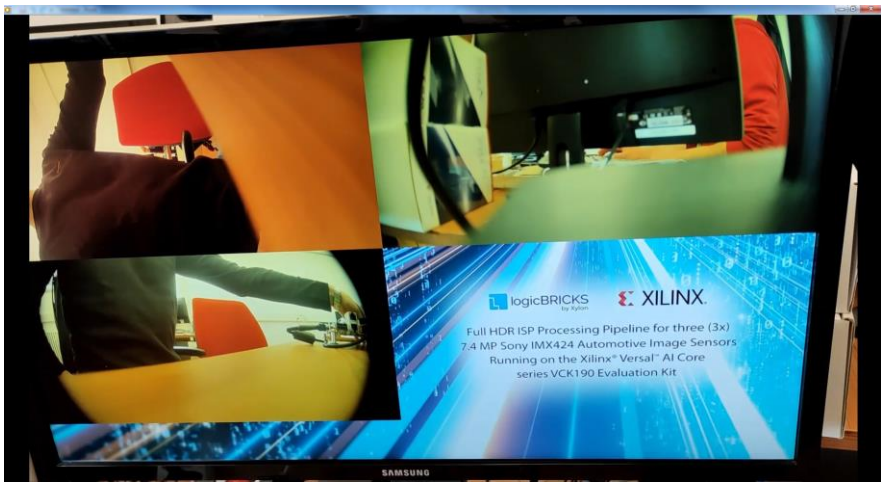

Figure 1: Display Output of the logiREF-ACAP-MULTICAM-ISP Framework

Features

- Complete ACAP HDR Image Signal Processing framework for multi-camera embedded applications with three 7.4MP (Ultra High Definition) video inputs from automotive video cameras
- Delivered as a part of Xylon's logiVID-ACAP-ISP evaluation kit
- Enables vision developers to quickly add their own algorithms to the provided infrastructure
- Jump-starts development and saves valuable design time
- Intended for use with next generation Maxim Integrated GMSL2 high-speed serial interface
- Fully compatible with Xylon's logiVID-ACAP-ISP HDR ISP evaluation kit based on the AMD-Xilinx Versal VCK190 Evaluation Board
- Includes licensed[1] Xylon logicBRICKS IP cores
- Design prepared for the following environment:
  - AMD-Xilinx Vivado Design Suite 2021.2
  - AMD-Xilinx Vitis Unified Software Platform
- Runs on Linux OS and includes logicBRICKS software drivers and demo applications
- HDMI™ display output with the AMD-Xilinx HDMI 1.4/2.0 Transmitter Subsystem[2] controlled via Xylon's DRM kernel driver
- Prepared for use with Sony LI-IMX424-GMSL2 Camera with the Sony IMX424 Image Sensor
- Design can easily be adapted for use with other UHD cameras
- Input video resolution: 3840x1920@30, Output video resolution: 3840x2160@30
- Full evaluation version available on request
- Documentation and Tech support (e-mail)

1. *Buyers of the logiVID-ACAP-ISP evaluation kit receive 3-month Xylon logicBRICKS seat evaluation licenses for the used logiISP, logiHDR, logiCVC-ML and logiWIN IP cores.*
2. *AMD-Xilinx licensed IP. Digital code vouchers provided by Xylon to buyers of the logiVID-ACAP-ISP HDR ISP evaluation kit for Versal ACAP.*

Table 1: ACAP HDR Image Signal Processing Framework Reference Design resources utilization

	Available in XCVC1902-VSVA2197-1	Used Resources in logiREF-ACAP-MULTICAM-ISP
Look-Up Tables (LUTs)	899,840	56.500 (~7.0%)
Flip-Flops (FFs)	1,799,680	82.300 (~5.0%)
Block RAM (36kB BRAM)	967	162.5 (~17.0%)
DSP Slices (MULT/DSP)	1,968	262 (~13.0%)

Applications

- Machine Vision and other vision applications, AR/VR, AD/ADAS, AI, guided robotics, drones etc.

General Description

The ACAP HDR Image Signal Processing Framework is intended to showcase a complete logicBRICKS IP suite implementation of High-Dynamic Range (HDR) Image Signal Processing (ISP) pipeline in an embedded design based on AMD-Xilinx ACAP programmable devices. The HDR ISP pipeline enables crisp camera video under altering and rough lighting conditions in next generation multi-channel embedded systems for use in automotive, surveillance, medical, aerospace and similar video and vision AI applications.

The logicBRICKS logiISP-UHD IP core enables parallel processing of multiple Ultra HD video inputs in different AMD-Xilinx devices, ranging from the small AMD-Xilinx Artix FPGAs to the latest AMD-Xilinx Versal Adaptive Compute Acceleration Platform (ACAP) devices. The design showcases how to connect high-quality inputs from automotive-grade cameras to on-board post-processing solutions or feed the stream to hardware-accelerated integrated neural networks running on this adaptive computing acceleration platform.

Key IP cores, the logiISP-UHD ISP and the logiHDR pipelines, support parallel processing of multiple video inputs, resolutions up to 7680x7680 (including the popular 4K2Kp60 video resolution), merging of two or three exposures, parallel pixel processing and different pixel formats. These IP cores for programmable logic implementations are supplemented with AWB and AE software libraries that use video statistics data collected at video inputs, software drivers, demo applications, reference SoC/ACAP designs, and bit-accurate C models.

The design framework implements three parallel video inputs from three 7.4Mpix Leopard Imaging IMX424 GMSL2 video cameras and the UHD display output. All video inputs are stored in the video memory, and by mean of on-board push buttons, the user can select each of them for the single camera or all cameras full screen display.

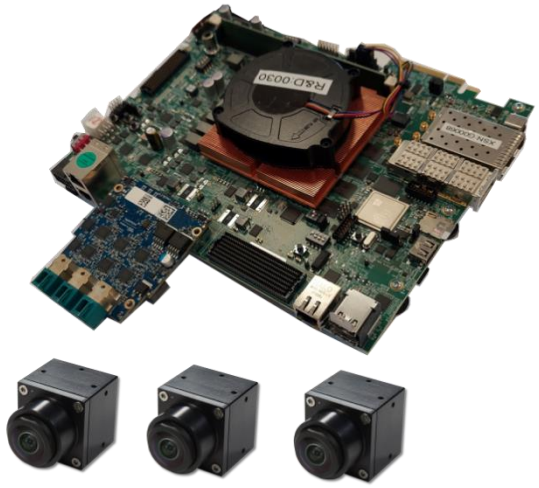

Figure 2: logiVID-ACAP-ISP HDR ISP Evaluation Kit and VCK190 Evaluation Kit

AMD-Xilinx Versal AI Core Series VCK190 evaluation kit must be purchased from AMD-Xilinx and distributers. Other logiVID-ACAP-ISP hardware components can be purchased directly from Xylon.

The logiREF-ACAP-MULTICAM-ISP reference design can be fully evaluated on the VCK190 with logiVID-ACAP-ISP HDR ISP evaluation kit designed by Xylon. This setup is based on the AMD-Xilinx Versal AI Core

Series VCK190 ACAP and includes Xylon's 12-Ch GMSL2 deserializer FMC module, three Leopard Imaging video cameras with the Sony IMX424 image sensor and GMSL2 link (LI-IMX424-GMSL2).

Each LI-IMX424-GMSL2 video camera is connected to its own GMSL2 deserializer device on Xylon's GMSL2 deserializer FMC module. Each of these deserializer devices drives a 4-lane MIPI port (interface) at a 800 Mbps per lane transfer rate.

All logicBRICKS IP cores are supplied with appropriate Linux software drivers. The provided video capture and display demo applications run in Linux OS.

If you are interested in AMD-Xilinx MPSoC implementations of the logicBRICKS HDR ISP pipelines, please contact Xylon at info@logicbricks or visit our website to learn more about our current offerings:

https://www.logicbricks.com/Solutions/Xylon-HDR-ISP.aspx

To download the evaluation version of the logiREF-ACAP-MULTICAM-ISP ACAP HDR Image Signal Processing Framework Reference Design or to purchase it, please visit our online catalog:

http://www.logicbricks.com/Products/logiREF-ACAP-MULTICAM-ISP.aspx

Figure 3: logiVID-ACAP-ISP HDR ISP evaluation kit and VCK190 evaluation kit

To learn more about the logiVID-ACAP-ISP HDR ISP evaluation kit, please visit:
https://www.logicbricks.com/Solutions/Xylon-ACAP-Vision-Development-Kits.aspx

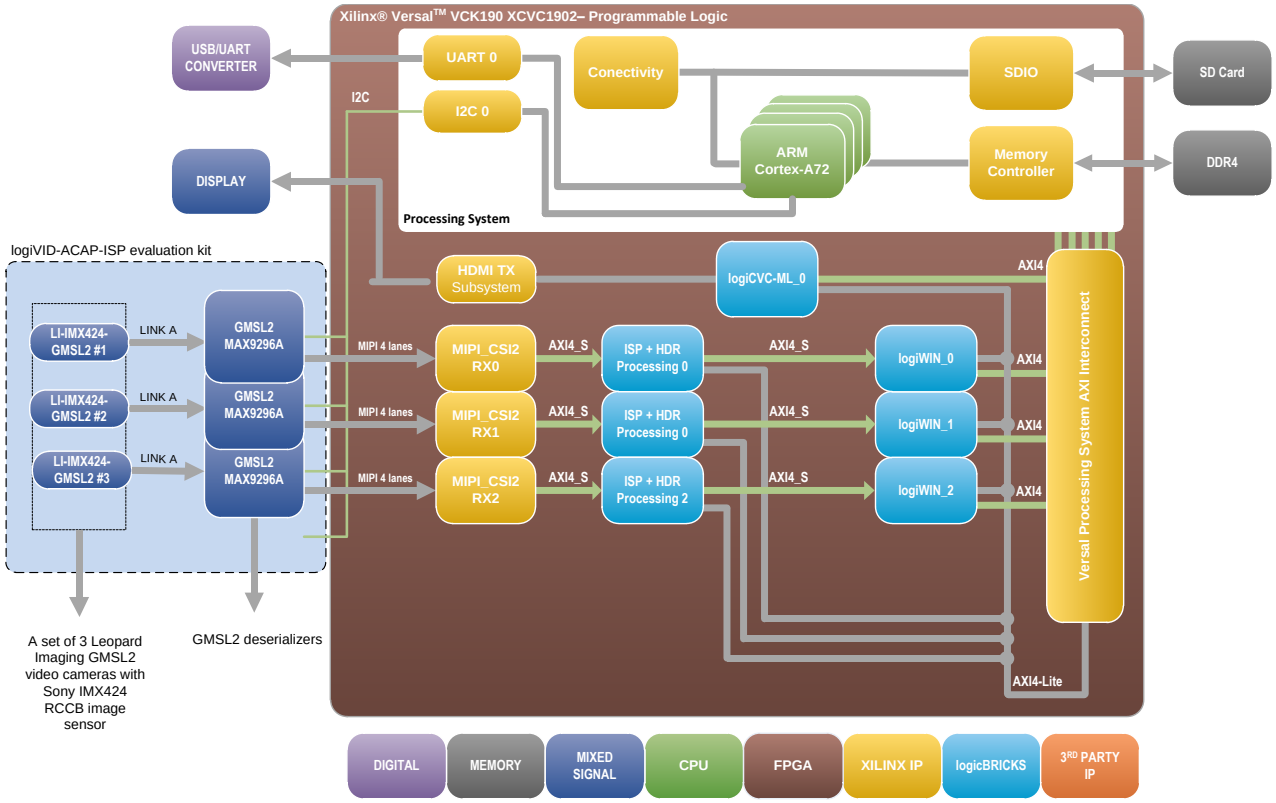

Figure 4: Subsystem Block Diagram for logiREF-ACAP-MULTICAM-ISP reference design

Reference Design Content

Hardware Design Files

- Hardware description file (XSA) as Vivado export of the reference design that allows for instant design check-ups and software changes in Vitis and PetaLinux environment
- Reference design prepared for the AMD-Xilinx Vivado Design Suite (script-based)
- AMD-Xilinx HDMI 1.4/2.0 Transmitter Subsystem IP
- Xylon's evaluation logicBRICKS IP cores:
    - Evaluation IP Cores have run-time limited operations and require occasional power down to restore functionality
    - logiISP-UHD Image Signal Processing UltraHD Pipeline
    - logiHDR High Dynamic Range Pipeline
    - logiCVC-ML Compact Multilayer Video Controller
    - logiWIN Versatile Video Input
    - License-free Xylon Utility IP cores

Software

- Vitis workspace files with Linux demo application projects
- Linux demo application sources
- PetaLinux 2021.2 project files
- Xylon specific software drivers and libraries

Binaries

- Precompiled SD card image for the fastest demo startup
- Xylon startup script
- Initialization files for Xylon's GMSL2 deserializer FMC module and cameras
- Xylon background image

Recommended Design Experience

Users that want to make changes on the provided designs should have experience in the following areas:

- AMD-Xilinx design tools (Vivado, Vitis, and PetaLinux)
- C/C++ programming
- Embedded hardware and software design

All logicBRICKS IP cores provided with the design framework are fully compatible with AMD-Xilinx's implementation tools and their use does not require any particular skillset beyond general AMD-Xilinx tools knowledge.

Related Xylon Products

The logiVID-ACAP-ISP HDR ISP evaluation kit for Versal ACAP provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP processing framework reference design and to efficiently develop multi-camera vision applications on AMD-Xilinx Versal devices. The complete hardware platform includes a Xylon 12-Ch GMSL2 deserializer FMC module, three LI-IMX424-GMSL2 Leopard Imaging video cameras and the necessary cables to get everything working. The evaluation kit supports HDMI video output to an external monitor.

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiVID-ACAP-ISP.aspx

The logiISP-ZU-GMSL2 HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to efficiently develop multi-camera vision applications on AMD-Xilinx's Zynq UltraScale+ MPSoC devices.The complete hardware platform includes four of Xylon's 2.3MP automotive video cameras with the raw Bayer video output and supports the HDMI video output to control a monitor.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiISP-ZU-GMSL2.aspx

The logiISP-UHD is an Ultra High Definition (UHD) ISP pipeline designed for digital processing and image quality enhancements of raw image data from video sensors. The logiISP-UHD accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data, manipulated video data formats and color domains…:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiISP.aspx

The logiHDR is an Ultra High Definition (UHD) HDR pipeline designed for digital processing and image quality enhancements of raw image data from HDR sensors. The logiHDR extracts maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by direct sunlight and objects placed in extreme shades:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHDR.aspx

Xylon provides software Auto White Balance (AWB) and Auto Exposure (AE) libraries for use with the logiISP-UHD IP core. To get more information about these products, please contact Xylon:

Email: info@logicbricks.com

Ordering Information

Products are available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on AMD-Xilinx programmable logic or development system software, contact your local AMD-Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00	17.10.2022.	Initial public release.