logiREF-DFX-IDF Dynamic Function eXchange Design Framework with Isolation Design Flow

February 23rd, 2022 | Data Sheet | Version: 1.0

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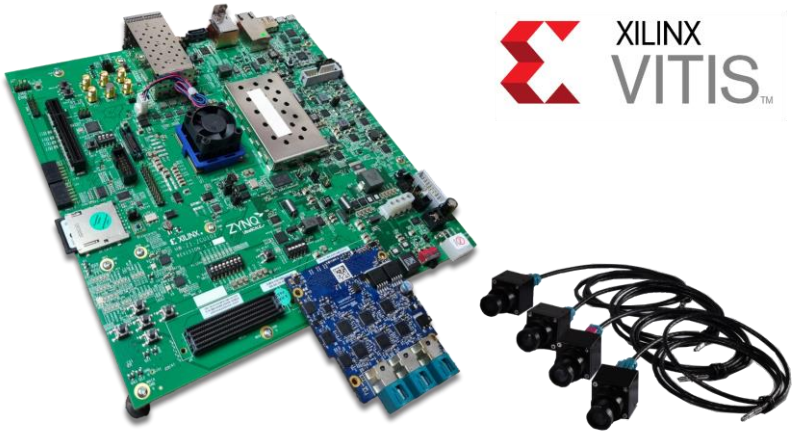

Figure 1: The Framework is part of the Xylon logiVID-ZU Vision Development Kit

Features

- The complete video design framework to explain and demonstrate Xilinx's Dynamic Function eXchange (DFX)
- The DFX enables features swapping by reconfiguring parts of a continually operating programmable FPGA/SoC chip
- Fail-safe demo chip designed through the Isolation Design Flow (IDF)
- Includes the Soft Error Mitigation (SEM) IP Core to demonstrate improved functional safety
- Design is fully compatible with the Xylon logiVID-ZU Vision Development Kit based on the Xilinx® Zynq® UltraScale+™ MPSoC
- Demonstrates reconfigurable video filtering on four video channels coming from four 2.3MP HDR cameras
- Video filters implemented by Xilinx Vitis™ Video Library HLS functions: Sobel, CCM Green, No Filter
- The logiVID-ZU kit includes licensed logicBRICKS by Xylon® IP Cores[1]
- Prepared for the following environment:
  - Xilinx Vivado® ML Design Suite 2021.1
  - Vitis Unified Software Platform
- Runs on Linux OS and includes logicBRICKS software drivers and demo applications
- HDMI® display output with the Xilinx HDMI 1.4/2.0 Transmitter Subsystem controlled via Xylon's DRM kernel driver[2]
- Full evaluation version available online
- Documentation and Tech support (e-mail)

1 *Included 1-year Xylon Low-Volume IP Program (LVIP) seat licenses for used Xylon logicBRICKS IP cores.*

2 *Licensed Xilinx IP core. Digital code vouchers provided by Xylon to buyers of the reference design or the logiVID-ZU kit.*

Applications

- Automotive AD/ADAS, guided robotics, drones, machine vision, AR/VR and other vision applications
- Demonstrated tools and techniques can be applied in all other applications that may benefit from Dynamic Function eXchange and Isolation Design Flow

Family (Device)	F (MHz)			LUT	FF	IOB[2]	BRAM	MULT/ DSP48/E	PLL / MMCM	BUFG	GTx	Design Tools
	mclk[4]	vclk[4]	rclk									
Zynq UltraScale+ (XCZU9EG-2)	(200/200)	(150/200)	100	98048	123892	48	265	177	1/2	27	0	Vivado ML 2021.1
Zynq UltraScale+ (XCZU9EG-2)	(200/200)	(150/200)	100	99472	123980	48	265	177	1/2	27	0	Vivado ML 2021.1
Zynq UltraScale+ (XCZU9EG-2)	(200/200)	(150/200)	100	103244	127084	48	283	177	1/2	27	0	Vivado ML 2021.1

Table 1: logiREF-DFX-IDF Reference Design Programmable Logic Utilization

1. Assuming the following configuration: AXI Stream, RGB output, 32-bit AXI4-Lite register interface, 64-bit AXI4 memory interface with max. burst size of 64 words, scaling in both directions with multipliers (DSP48s), output stride set to 2048 pixels
2. Assuming only video inputs are routed off-chip, register and memory interfaces are connected internally
3. Only burst size of 16 words is supported on HP ports in the Xilinx Zynq UltraScale+ MPSoC
4. logiCVC/logiWIN clock frequencies

General Description

The logiREF-DFX-IDF Design Framework enables users to quickly get a grasp on demonstrated key technologies: Dynamic Function eXchange, Isolation Design Flow and use of the SEM IP for increased design Functional Safety. The framework works on Xylon's logiVID-ZU hardware platform based on the Xilinx Zynq UltraScale+ MPSoC. This hardware platform is optimized for embedded multi-camera vision systems. However, the demonstrated principles, techniques and design solutions can be easily adapted for different application spaces and other Xilinx programmable devices.

The logiREF-DFX-IDF design framework includes the MPSoC design that processes HD video channels from four 2.3MP automotive cameras. Each video channel includes a reconfigurable partition (RP) of programmable logic that can be re-configured by different video filtering modules defined by a set of three partial BIT files provided for each RP. Processed video streams are displayed on the HDMI monitor attached to the Xilinx evaluation board. Demo users can choose between a single camera view and an all cameras tiled view. Also, each video channel can be independently processed by a reconfigurable Sobel filter, CCM Green, or no filter (RGB view). The demo also includes video error injection and its correction by an integrated SEM IP core.

Dynamic Function eXchange (DFX) is the ability to deliver new capabilities to silicon on demand, while critical functions remain running. In other words, the DFX enables features swapping by reconfiguring parts of a continually operating programmable FPGA/SoC chip. Reconfigurable blocks of programmable logic are dynamically modified by downloading partial bit files.

The Isolation Design Flow (IDF) enables designers to develop fail-safe single chip solutions that confine the fault to a single region of the chip – without affecting more than one function. It enables implementation of security- or safety-critical designs. The chip design is immune to single point failures (except power and ground). Isolated Regions (**Figure 2**) can be defined as RP reprogrammable partitions to confine faults on a single chip function (Region).

Flexibility of the existing design is taken one step further by utilizing Dynamic Function eXchange (DFX) and Isolation Design Flow (IDF) solutions together to allow modifications of operating FPGA design by loading partial BIT files defining video filtering examples. Demonstrated video filters are built by Vitis Vision Library HLS functions.

This increases system flexibility, reduces cost and size of the required hardware, while ensuring a fault-tolerant chip design with functional safety in mind.

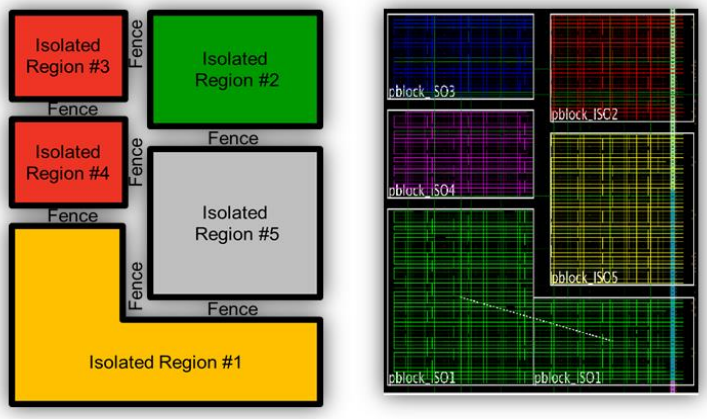

Figure 2: Graphical example of Isolated Regions ***(image from www.xilinx.com)***

The design comes with implemented Xilinx's Soft Error Mitigation IP (SEM), which is an automatically configured, pre-verified solution for detection and correction of errors in Configuration Memory of Xilinx FPGAs. SEM IP provides the ability to detect and correct single errors (SEU – Single Event Upset) in the configuration memory of programmable logic. The IP core is using ECC and CRC values associated with the configuration bitstream. In case of multiple configuration errors, the SEM IP signals the Processing System to initiate DFX reconfiguration of the isolated faulty chip region. The SEM IP can emulate SEU by injecting errors into configuration memory, and the framework uses it to demonstrate DFX + IDF capabilities.

Figure 3: Tiled, Full Screen and Error Injection Modes of the logiREF-DFX-IDF Design Framework

The logiREF-DFX-IDF Design Framework is specifically prepared for evaluation on the GMSL2 version of the logiVID-ZU MPSoC Vision Development Kit, shown in **Figure 4** below:

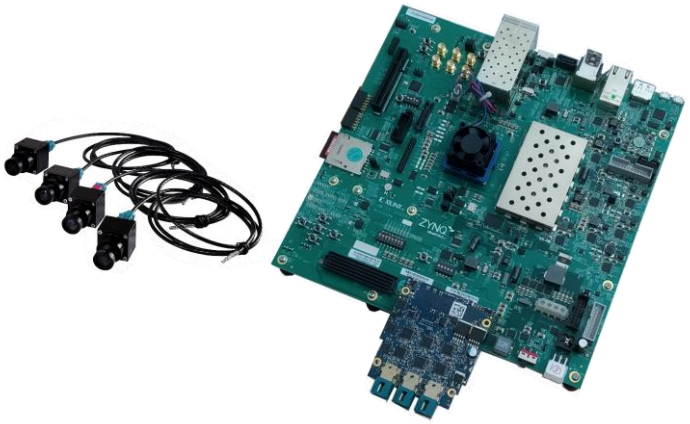

Figure 4: Xylon logiVID-ZU-GMSL2 Vision Development Kit

The complete hardware kit includes the Xilinx ZCU102 Evaluation Kit, Xylon 12-ch GMSL2 FMC video board, Xylon 2.3MP automotive video camera, Rosenberger® FAKRA cables, and power supply. To learn more about the logiVID-ZU platform, please check the datasheet:
https://www.logicbricks.com/Documentation/Datasheets/HW/logiVID-ZU_hds.pdf

The provided MPSoC design includes pre-verified and licensed Xylon logicBRICKS IP Cores. It is prepared for the 2021.1 versions of the Xilinx Vivado ML Design Suite & Xilinx Vitis Unified Software Platform.

All IP cores are supplied with appropriate Linux software drivers. The provided video capture and display demo applications run on the Linux operating system.

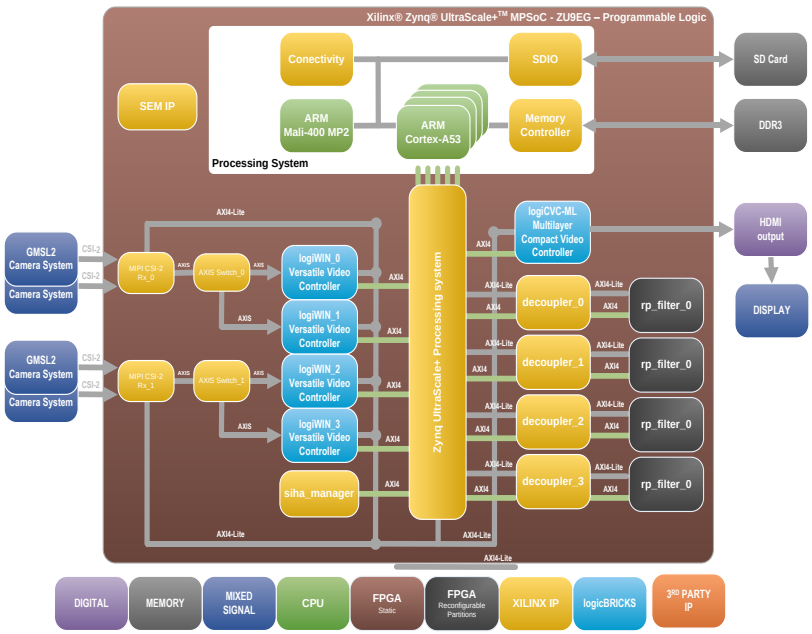

Figure 5: logiREF-DFX-IDF MPSoC Design Block Diagram

To download the evaluation version of the logiREF-DFX-IDS Video Design Framework, please visit our online catalog: http://www.logicbricks.com/Products/logiREF-DFX-IDS.aspx.

Framework Content

logiREF-DFX-IDS Design Framework for the Xilinx Vivado ML Design Suite:

Vitis platform

- Reference design prepared for Vitis Unified Software Platform
- Configuration bitstreams files for the programmable logic and Vitis export of the reference design that allows for instant design check-up and software changes
- Reference design prepared for Vivado ML 2021.1
- Xilinx HDMI 1.4/2.0 Transmitter Subsystem
- Xylon evaluation logicBRICKS IP cores:
  - logiCVC-ML Compact Multilayer Video Controller
  - logiWIN Versatile Video Input
- Xylon IP Cores that are not sold separately but only serve to augment this specific reference design:
  - TUSER-Trimmer

Software

- logiVIOF VideoIn-VideoOut library
- DFX-IDF Demo application sources
- Linux user space drivers with driver examples
- Bare-metal software drivers for logicBRICKS IP cores

Binaries

- FPGA bitstreams
- Linux binaries:
    - boot.bin
        - First Stage Boot Loader
        - Universal Boot Loader
        - FPGA
        - Platform Management Unit Firmware
    - image.ub
        - kernel image
        - device tree blob
        - minimal Root File System
    - Four Camera DFX-IDF demo

Recommended Design Experience

Users that want to make changes to the provided designs should have experience in the following areas:

- Xilinx design tools
- C programming
- Embedded hardware and software design

All logicBRICKS IP cores provided with the design framework are fully compatible with Xilinx implementation tools and their use does not require any particular skills beyond general Xilinx tools knowledge.

Related Xylon Products

The logiVID-ZU Vision Development Kit provides system designers with everything they need to efficiently develop multi-camera vision applications on the Xilinx Zynq UltraScale+ MPSoC devices. The kit includes a complete hardware platform that supports a single HDMI video output, and depending on the kit version, up to four inputs from Xylon GMSL2 or FPD-Link III video cameras, as well as the fully licensed logiADAK-VDF-ZU Video Design Framework (only with Xylon AR0231 cameras). Only the GMSL2 version of this kit is supported by the logiREF-DFX-IDF Design Framework. To learn more about this product, please contact Xylon or visit our website:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiVID-ZU.aspx

The logiADAK-VDF-ZU MPSoC IP Framework for Multi-Camera Vision Applications enables Xylon logiVID-ZU Vision Development Kit users to quickly utilize the logiVID-ZU hardware platform for development of embedded multi-camera vision systems. The framework includes pre-verified logicBRICKS reference designs for video capture from Xylon cameras, and the display output with an RGB overlay under the Linux operating system. To learn more about this product, please contact Xylon or visit our website:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiADAK-VDF-ZU.aspx

Ordering Information

The product is available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiREF-DFX-IDS.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00	23.02.2022.	Initial public release.