logiREF-DISP-MicroZed

Xylon logicBRICKS Video Display Reference Design for Xilinx® Zynq™-7000 All Programmable SoC based MicroZed™ from Avnet Electronics Marketing

User's Manual

Version: 1.00.a

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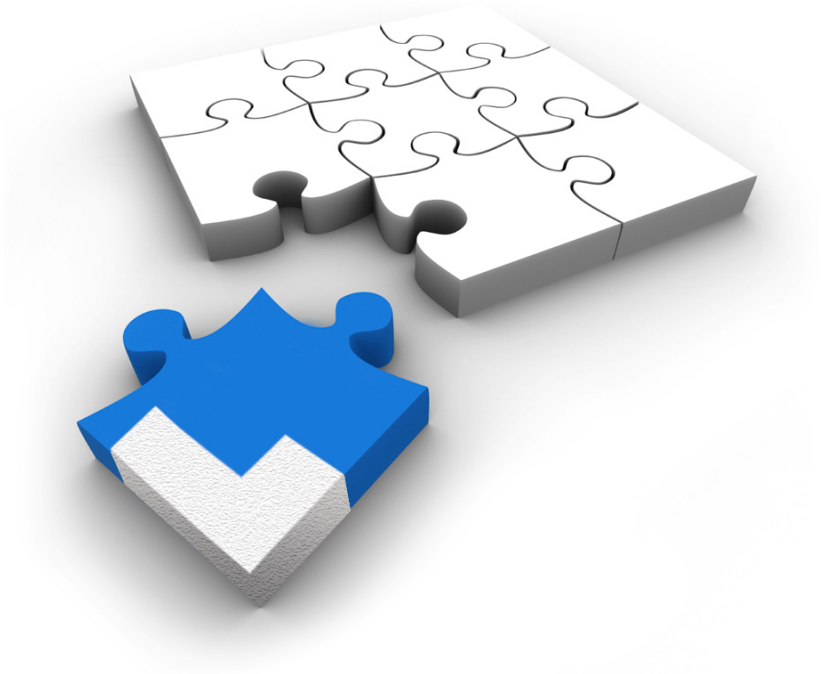

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1 INTRODUCTION

Xylon's logicBRICKS library of IP cores optimized for Xilinx programmable devices includes several graphics logicBRICKS IP cores for full range implementation of 2D and 3D Graphics Processing Units (GPU) on Xilinx Zynq-7000 All Programmable SoC and FPGAs.

This user's manual describes Xylon's video display reference design for the MicroZed from Avnet Electronics Marketing. The MicroZed is a low-cost development board based on the Xilinx Zynq-7000 All Programmable SoC which is designed as an embeddable System-on-Module (SOM) and should be combined with a carrier card and a 7" Zed Touch Display Kit in order to run Xylon reference design.

The provided demo showcases ilixi user interface (UI) toolkit for Direct Frame Buffer (DirectFB) graphics library for Linux based operating systems (OS). The UI works as a demo application launcher controlled by a capacitive touchscreen.

Figure 1.1 The MicroZed Development Kit Running Xylon's Video Display Demo

The reference design includes evaluation logiCVC-ML multi-layered display controller IP core with advanced blending capabilities and hardware design files prepared for Xilinx Vivado™ design suite. It also includes complete Linux OS image, software drivers, demo applications and documentation.

System designers can leverage the flexibility and scalability of logiCVC-ML IP core and software to speed up their development cycle. The reference design comes with an evaluation logicBRICKS license that enables designers to re-configure the display controller IP core and customize it for specific needs, i.e. for different LCD display control. Software designers can develop Linux applications for their product before target hardware is available and hardware designers can customize the provided logicBRICKS design to closely fit to their requirements.

logicBRICKS IP cores can be delivered with software drivers for the most popular operating systems: Linux, Microsoft® Windows® Embedded Compact 7 and Android™. For more information about Xylon software support for graphics IP cores, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx.

Besides the reference design for the MicroZed evaluation kit, Xylon also provides reference designs for the ZedBoard™ evaluation kit from Avnet Electronics Marketing and other Xilinx Zynq-7000 AP SoC based evaluation/development kits:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx.

1.1 Hardware Platform

The logiREF-DISP-MicroZed Video Display Reference Design works with the following hardware boards from Avnet Electronics Marketing:

- MicroZed Evaluation Kit (Part Number: AES-Z7MB-7Z010-G)
- I/O Carrier Card (Part Number: AES-MBCC-IO-G)
- 7-inch Zed Touch Display Kit (Part Number:AES-ALI2-ZED-G)

For full hardware setup instructions, please read the section 6.5 Set Up the MicroZed for Use with Precompiled Linux Demos from the SD Card.

1.2 Design Deliverables

1.2.1 Hardware design files

- Configuration bitstream file for the programmable logic and the SDK export of the reference design that allows an immediate start and software changes
- MicroZed reference SoC design prepared for Vivado implementation tools
- Xylon evaluation logicBRICKS IP cores:
    - logiCVC-ML Compact Multilayer Video Controller

1.2.2 Software

- Zynq FSBL sources and the Xilinx SDK project – custom version for standalone applications
- Linux Frame Buffer driver for the logiCVC-ML IP core (by Xylon)
- DirectFB driver for the logiCVC-ML IP core (by Xylon)

1.2.3 Binaries

- First Stage Bootloader (FSBL)
- Linux binaries:
    - u-boot, dts, dtb, root file system
    - uImage – kernel with the frame buffer driver for the logiCVC-ML IP core
    - DirectFB library and DirectFB examples using Xylon DirectFB driver

1.3 Graphics Demo Preview

Please check Xylon's Video Gallery to see graphics demo applications running on the MicroZed development kit:

http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Demos-MicroZed-Kit.aspx.

2 LOGICBRICKS IP CORES

2.1 About logicBRICKS IP Library

Xylon's logicBRICKS IP core library provides IP cores optimized for Xilinx FPGA and Zynq-7000 All Programmable SoC. logicBRICKS IP cores shorten development time and enable fast design of complex embedded systems based on Xilinx programmable devices.

The key features of the logicBRICKS IP cores are:

- Compatibility with the Vivado* design suit and Xilinx Platform Studio (XPS). logicBRICKS can be used in the same way as Xilinx IP cores from the Vivado IP catalog, and require no skills beyond general tools knowledge
- Each logicBRICKS IP core comes with the extensive documentation and can be evaluated on reference hardware platforms
- Broad software support – from bare-metal software drivers to standard software drivers for different operating systems (OS). Standard software support allows graphics designers and software developers to use logicBRICKS in a familiar and comfortable way
- Xylon assures skilled technical support
- A number of logicBRICKS IP cores can be quickly purchase and licensed through Xylon's web shop: http://www.logicbricks.com/Products/IP-Cores.aspx

** Currently supported IP cores are the logiCVC-ML Compact Multi-Layered Video Controller and the logiSDHC SD Card Host Controller. Xylon currently work on porting the whole logicBRICKS IP library to Vivado design suite.*

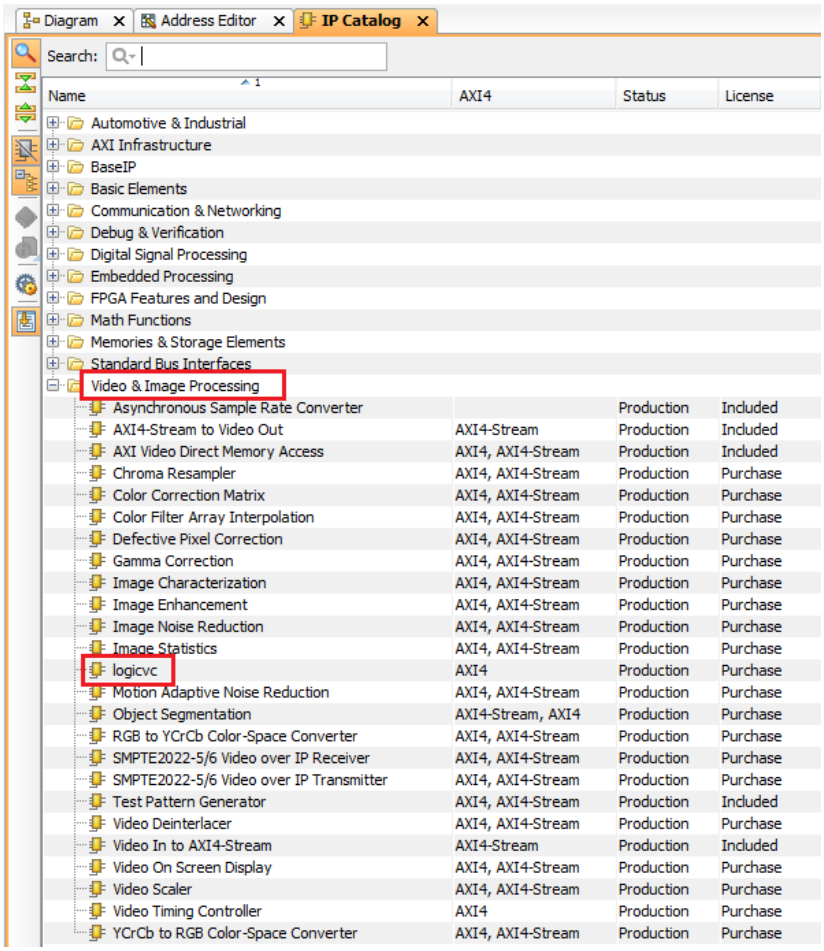


Figure 2.1 logiCVC-ML IP Core Imported into the Vivado IP Catalog

The Figure 2.1 shows imported logiCVC-ML IP core into Xilinx development software, while the Figure 2.2 shows its configuration GUI that allows for customizations.

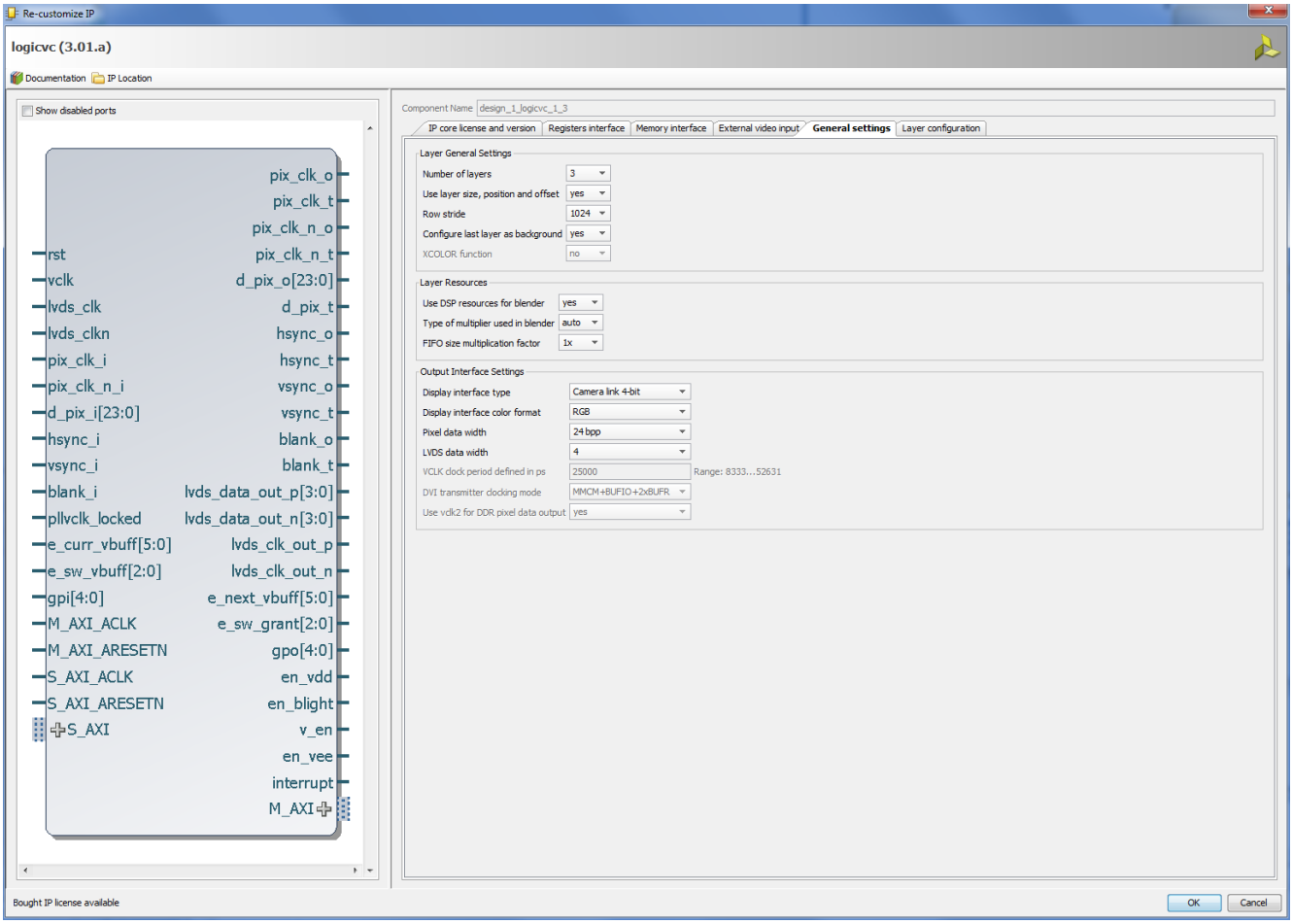


Figure 2.2 An example of logiCVC-ML IP Configuration GUI

Click on the Product Guide PDF icon under Documentation section in the GUI opens the User's Manual document of the logicBRICKS IP Core!

2.2 Evaluation logicBRICKS IP Cores

Xylon offers free evaluation logicBRICKS IP cores which enable full hardware evaluation:

- Use in the Vivado design suite
- IP parameterization through the configuration GUI interface
- Bitstream generation

The logicBRICKS evaluation IP cores are run-time limited and cease to function after some time. Proper operation can be restored by reloading the bitstream. Besides this run-time limitation, there are no other functional differences between the evaluation and fully licensed logicBRICKS IP cores.

Evaluation logicBRICKS IP cores are distributed as parts of the Xylon reference designs: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx.

Specific IP cores can be downloaded from Xylon's web shop: http://www.logicbricks.com/Products/IP-Cores.aspx.

2.3 logicBRICKS IP Cores Used in This Design

2.3.1 logiCVC-ML Compact Multilayer Video Controller

The logiCVC-ML IP core is an advanced video display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems with Xilinx Zynq-7000 All Programmable SoC and FPGAs.This IP core is the cornerstone of all 2D and 3D GPUs. Though its main function is to provide flexible display control, it also includes a level of hardware acceleration: alpha blending, panning, buffering of multiple frames, etc…

The logiCVC-ML IP core enables enables easy mixing and blending of multiple video inputs with the overlaying HMI. The blending is HW accelerated and need no CPU time! The IP core also implements means for video input and output synchronization.

- Supports all Xilinx FPGA families
- Software support for Linux, Android and Microsoft Windows Embadded Compact OS
- Supports LCD and CRT displays (easily tailored for special display types)
- 64x1 to 2048x2048 display resolutions
- Support for higher display resolutions available on request
- Supports up to 5 layers; the last one configurable as a background layer
- Configurable layers' size, position and offset
- Alpha blending and color keyed transparency
- Pixel, layer, or color lookup table (CLUT) alpha blending mode can be independently set for each layer
- Packed pixel layer memory organization – pixel color depth 8-bpp, 8-bpp using CLUT, 16-bpp Hi-color RGB565 and 24-bpp True-color RGB888
- Configurable CoreConnect™ PLBv4.6, Xylon XMB or ARM® AMBA® AXI4 memory interface data width (32, 64 or 128)
- Programmable layer memory base address and stride
- Simple programming due to small number of control registers
- Support for multiple output formats:
    - Parallel display data bus: 12x2-bit, 15-bit, 16-bit, 18-bit or 24-bit
    - Digital Video ITU-656: PAL and NTSC
    - LVDS output format: 3 or 4 data pairs plus clock
    - Camera link output format: 4 data pairs plus clock

    - DVI output format
    - YCbCr 4:4:4 or 4:2:2 output format
- Supports synchronization to external parallel input
- HW cursors
- Versatile and programmable sync signals timing
- Double/triple buffering enables flicker-free reproduction
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Vivado design suite and Xilinx Platform Studio (XPS)

More info: http://www.logicbricks.com/Products/logiCVC-ML.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCVC-ML_hds.pdf

3 GET AND INSTALL THE REFERENCE DESIGN

Only registered logicBRICKS users can download logicBRICKS reference designs. Unregistered users will be re-directed to the User Login page. The download link is automatically sent by an e-mail, which means that the registration process requires an access to the e-mail account.

A quick access to specific reference design is also possible through the main downloads navigation page:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx.

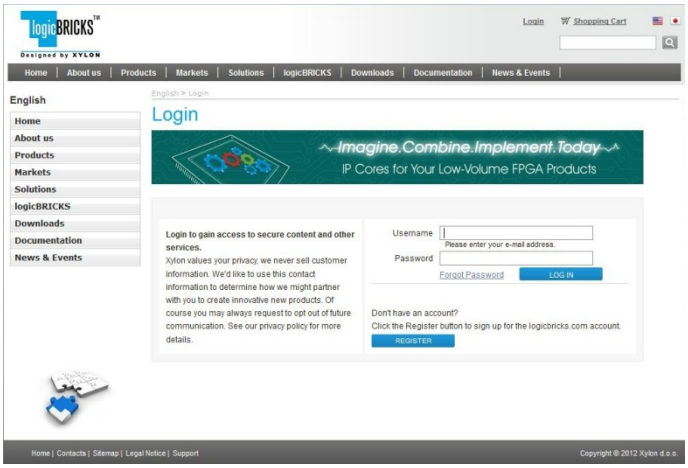
Xylon logicBRICKS reference designs can be downloaded as self-extracting installers compatible with Microsoft Windows operating systems, or as a cross-platform Java JAR self-extracting installer.

Xylon offers several logicBRICKS reference designs for different hardware platforms. Short descriptions of all Xylon logicBRICKS reference designs can be found at:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

3.1 Registration Process

Registration is very quick and simple. If you experience any troubles during the registration process, please contact Xylon Technical Support Service – support@logicbricks.com.



Step 1

If you are the registered logicBRICKS user, please type-in your Username and Password. Unregistered users should click on the Register button, which will open the registration form.

Figure 3.1 Registration Process – Step 1

Figure 3.2 Registration Process – Step 2

Step 2

Unregistered users should fill-in the registration form from the Figure 3.2. Please take care on required form's fields. Your Username is an actual e-mail account used for communication with Xylon logicBRICKS. Xylon accepts only valid company e-mail accounts.

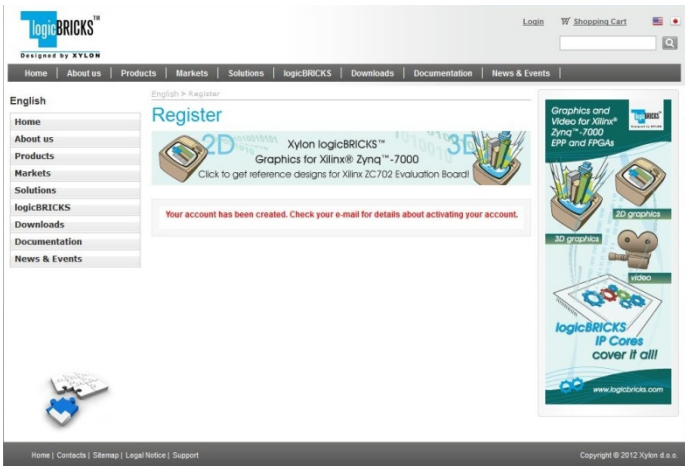


Figure 3.3 Regsitration Process – Step 3

Step 3

As soon as your registration form gets accepted by Xylon, you get a confirmation message. Please check your e-mail to find a link that activates your logicBRICKS account. If you do not get the confirmation message in several minutes, please contact Xylon support.

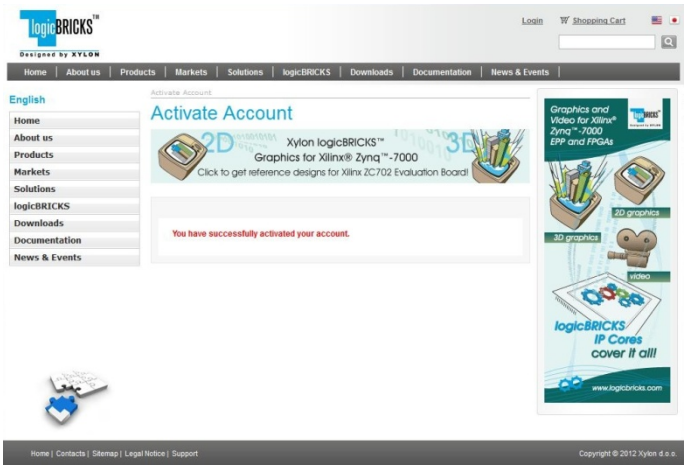


Figure 3.4 Registration Process – Step 4

Step 4

Click on the logicBRICKS web account activation link in the received e-mail, and you will get the confirmation status message. Please login to proceed.

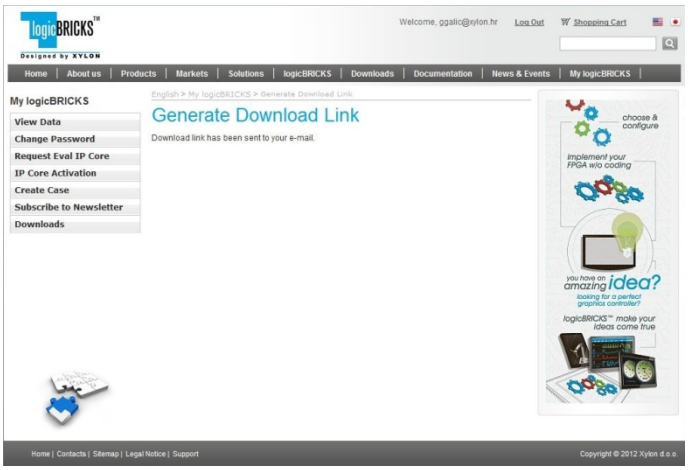


Figure 3.5 Registration Process – Step 5

Step 5

As soon as you select an appropriate logicBRICKS reference design and installer for your operating system from the Downloads Navigation Page (link bellow), you will get an e-mail with the download link for the selected reference design installation.

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

3.2 Installation Process

Installation process is quick and easy. Start the self-extracting installer (JAR or EXE). At the beginning, you will be requested to accept the license agreement – Figure 3.6.

Users of the self-extracting JAR installer must have a copy of the JRE (Java Runtime Environment) version 6 or higher on your system to run Java applications and applets!

If you agree with the conditions from the license agreement, click NEXT and select the installation path for your logicBRICKS reference design – Figure 3.7.

The installation process takes several minutes. It generates the directory structure described in the section 3.3 Directory Structure.

Figure 3.6 Installation Process – Step 1

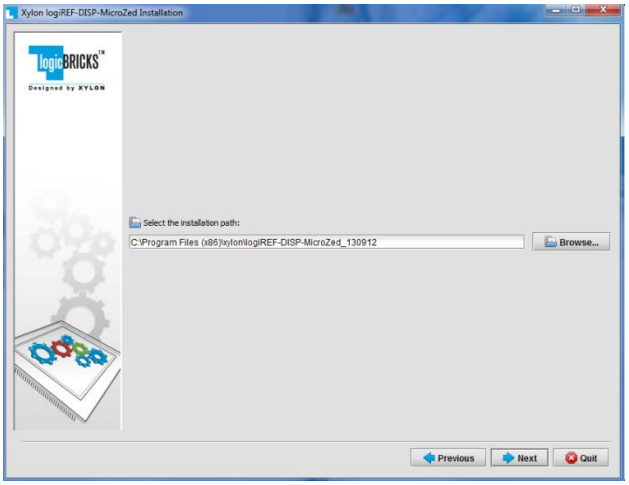


Figure 3.7 Installation Process – Step 2

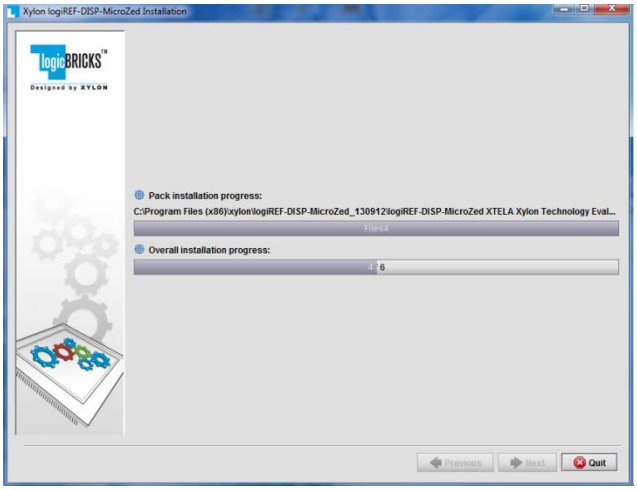


Figure 3.8 Installation Process – Step 3

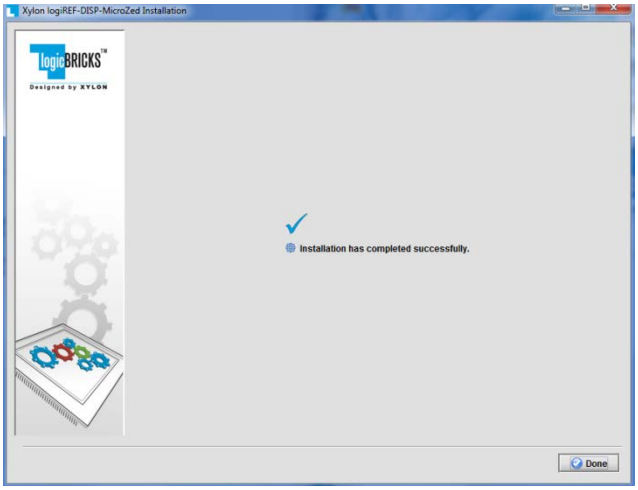


Figure 3.9 Installation Process – Step 4

3.3 Directory Structure

Figure 3.10 gives a top level view of the directories and files included with the logiREF-DISP-MicroZed reference design for the MicroZed development kit. Table 3.1 provides quick explanations of directories' purpose.

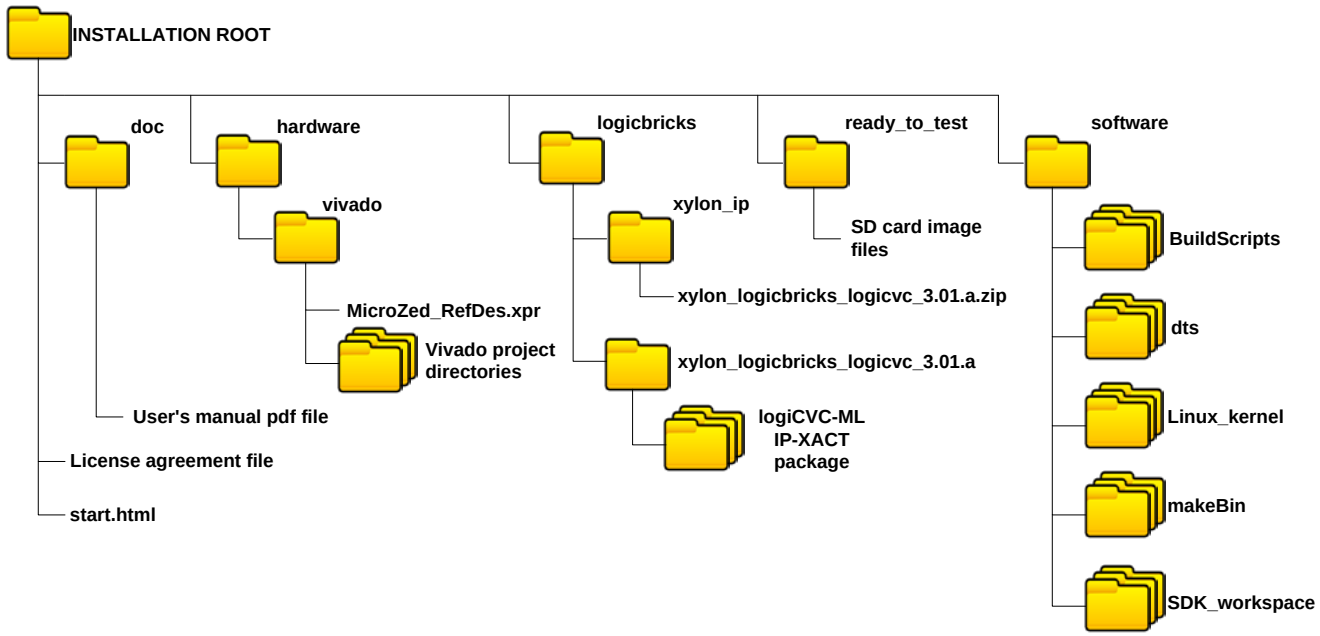


Figure 3.10 Directory Structure

Directory		Purpose/Content
INSTALLATION ROOT		Root directory of the installation package, also includes Technology Evaluation License agreement file; the directory also contains start.html file, the jump-start navigation page through the reference design
doc		The directory contains MicroZed reference design User's Manual pdf file
hardware		This directory contains the complete XPS project
	Project file	Project file MicroZed_RefDes.xpr for opening the reference design project in Vivado tool
	Design directories	Vivado project related directories
logicbricks		The directory contains logicBRICK IP cores
	logiCVC-ML IP-XACT zip package	xylon_logicbricks_logicvc_3.01.a.zip is an IP-XACT package file (VLNV naming convention)
	logiCVC-ML IP-XACT package files	Unzipped IP-XACT package files used in Vivado project
ready_to_test		The directory contains all the necessary image files for SD card (binaries) for the reference design demo "plug and play"
software		The directory contains software files for the reference design
	BuildScripts	The directory contains scripts for building DirectFB, ilixi and qt
	dts	Linux device tree configuration file
	Linux_kernel	The directory contains: • Linux Kernel patch with modifications to Xylon's xylonfb driver, • patch that contains support for TMG120 touch-screen displays, • ramdisk image and script necessary for building uramdisk (contains intial filesystem), • instructions for building Linux Kernel and uramdisk.
	makeBin	Utility scripts for creating boot.bin file, fsbl.elf (first stage boot loader binary), system.bit (configuration bitstream file), u_boot.elf
	SDK_workspace	Xilinx SDK workspace folder for building bare-metal applications

Table 3.1 Explanation of Directories in logiREF-DISP-MicroZed Reference Design

4 LOGIREF-DISP-MICROZED DESIGN

The logiREF-DISP-MicroZed is the pre-verified Xylon's reference design that showcases logicBRICKS video display controller IP core – logiCVC-ML. Designers can use the provided evaluation logicBRICKS IP core to quickly customize and build a working video controller engine for their Zynq-7000 AP SoC design through an easy plug-and-play Vivado IP Integrator design flow in a small and efficient video display control that uses just a fraction of programmable logic in the smallest Z7010 Zynq-7000 device.

Hardware designers that are familiar with Xilinx design tools can immediately start designing with logicBRICKS. An easy to use Vivado IP Integrator GUI interface enables a user-friendly (IP drag and drop) design of complex embedded systems with no need for HDL coding. Additionally, the Vivado IP Integrator GUI allows IP tuning of slice consumptions and feature sets definitions.

Provided software drivers include standard Linux FrameBuffer driver and Direct Frame Buffer (DirectFB) graphics library. Standard software drivers enable software developers to work fast and efficiently with popular graphic libraries, widget toolkits and familiar development tools.

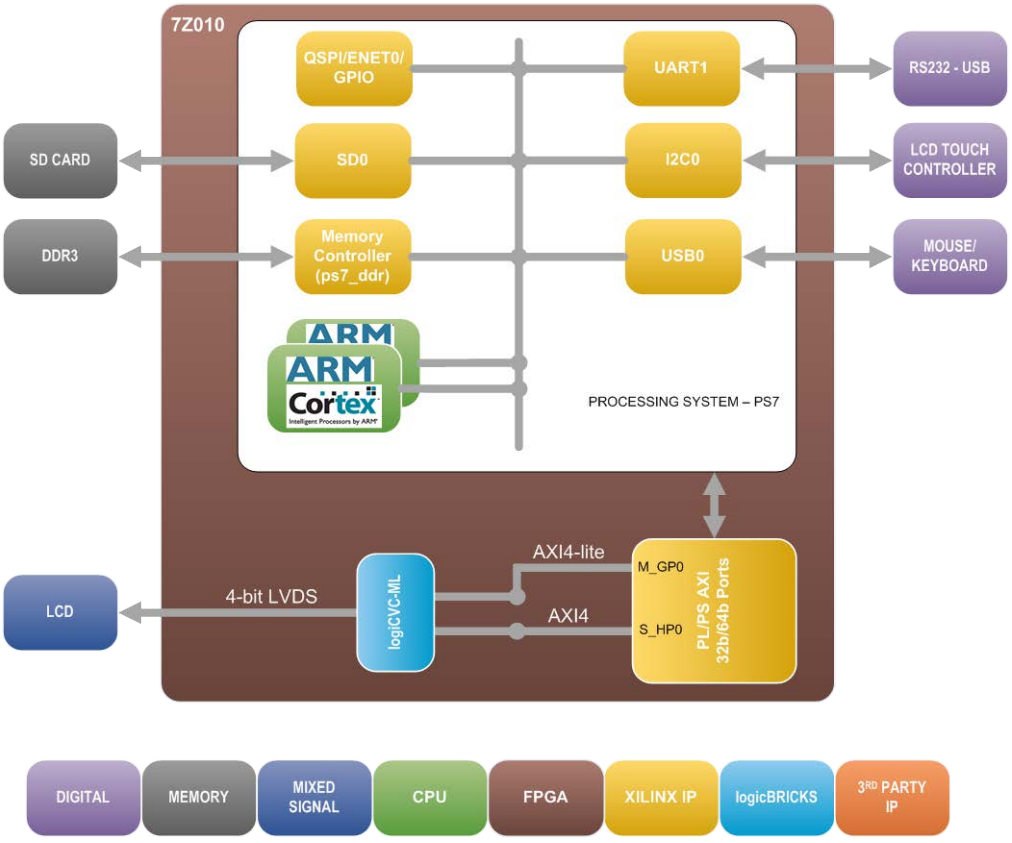


Figure 4.1 logiREF-DISP-MicroZed Reference Design – Block Diagram

(Clock Generator Module and other utility IP cores are not shown)

Figure 4.1 shows the simplified block diagram of the logiREF-DISP-MicroZed reference design. Design clocking structures are not shown. Please read the section 6. VIDEO OUTPUT CLOCKING and explore the design files to understand the clocking structure.

The logiCVC-ML Compact Multilayer Video Controller IP core is an advanced display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems based on Xilinx programmable technology. Though its main function is to provide flexible display control, it also includes a level of hardware acceleration: alpha blending, panning, buffering of multiple frames, etc. The logiCVC-ML IP core can directly drive an industrial LVDS interface displays, such as the one used in MicroZed development platform set.

The memory subsystem is an essential part of any graphics based system. It must ensure enough storage space for GUI elements and application code and a fast interface to assure enough memory bandwidth for a flicker-free display output. The MicroZed includes two 16-bit DDR3 memories connected as one 1024 MB (1 GB) 32-bit memory module. The memory is connected to the hard-coded memory controller in the Zynq-7000 AP SoC Processor Subsystem (PS).

4.1 Design Customization

The provided reference design can be customized in different ways. For example:

- change logicBRICKS IP settings, i.e. change number of graphics layers controlled by the logiCVC-ML display controller IP core;
- add more instances of logicBRICKS IP cores, i.e. add second logiCVC-ML IP core and drive two displays with different graphics content;
- add your own or third-party IP cores to various combinations of logicBRICKS IP cores;
- …

Architecture featuring only the logiCVC-ML display controller IP core is a configuration that provides no graphics acceleration in the programmable logic and all graphic contents must be fully drawn by the Processing Subsystem (PS). The consumption of programmable logic resources is minimal.

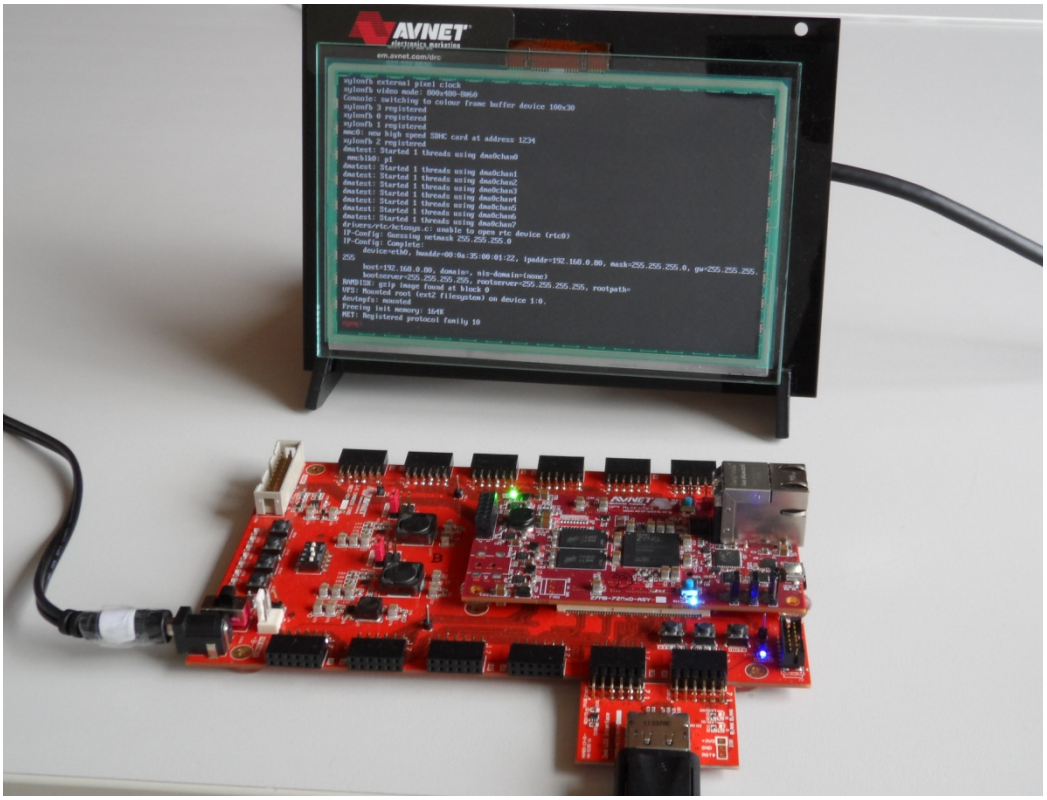


Figure 4.2 The MicroZed Running Linux Console

4.2 Memory Layout

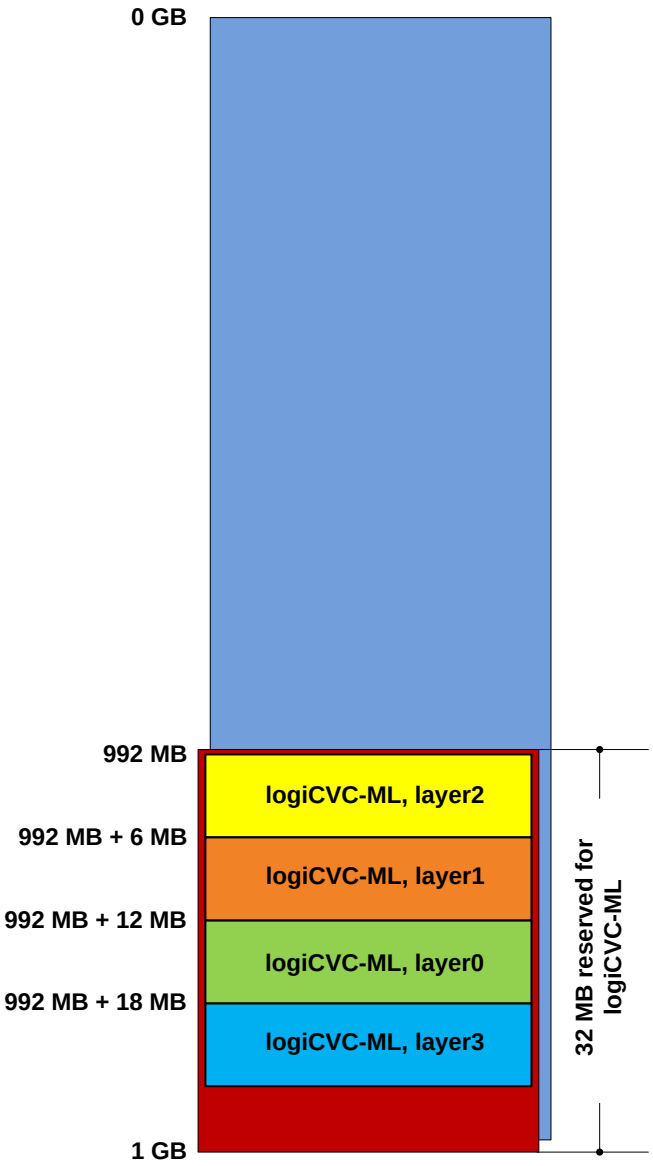


Figure 4.3 logiREF-DISP-MicroZed Memory Layout

IP Core	Memory Access [MB]	Memory Stride [pixels]	Display Memory [HxV pixels]
logiCVC-ML	992 – 1023	1024	up to 800x480

Table 5.1 logicBRICKS IP Cores' Memory Addressing

4.3 Restoring Zynq-7000 Design from Xylon Deliverables

Xylon provides all necessary design files for full Vivado project restore. Currently used implementation tool is Vivado 2013.2.

The `MicroZed_RefDes.xpr` file from your installation folder is the Vivado project file that opens the project. Open this file with the Vivado tool and explore the design – Figure 4.4.

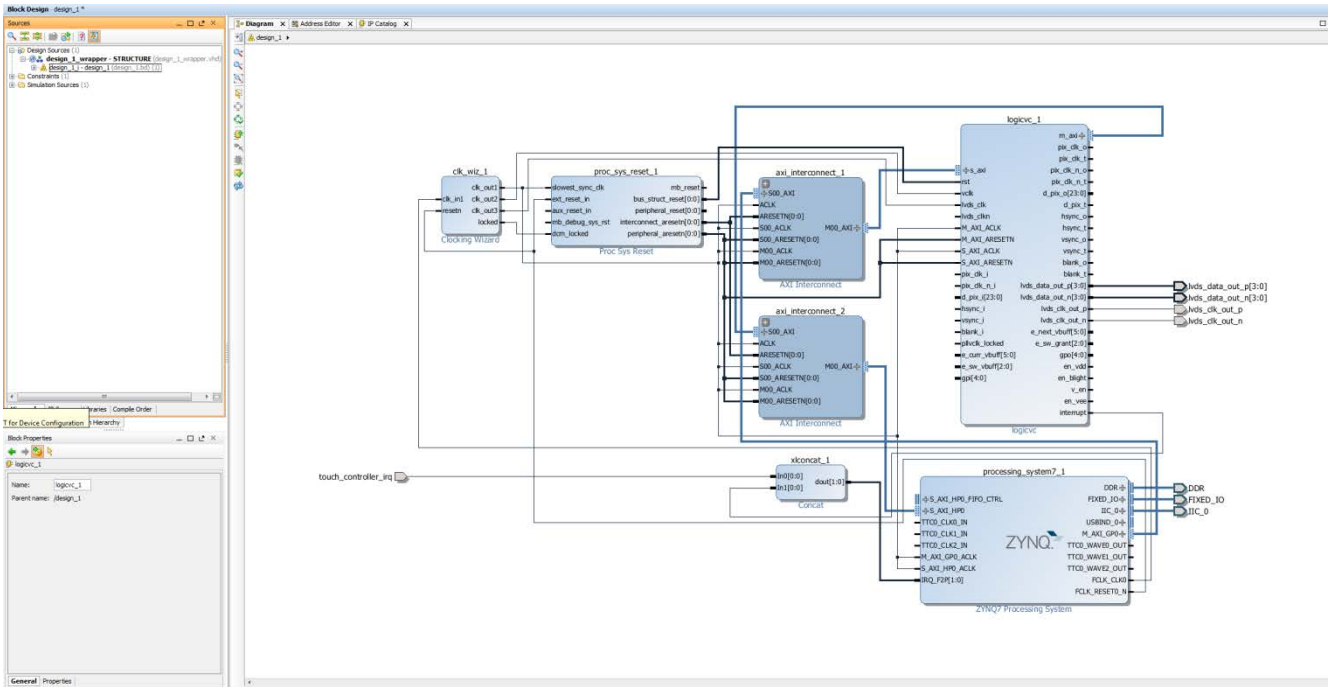


Figure 4.4 Vivado IP Integrator View – logiREF-DISP-MicroZed project

To access logicBRICKS IP cores' user's manuals, click on the corresponding IP core's cell to designate it, and then double click on it to open the customization GUI, and click on the PDF icon to open the document. The Product Guide PDF icon is located under Documentation tab.

logicBRICKS User's Manuals contain all necessary information about the IP cores' features, architecture, registers, modes of operation, etc.

5 VIDEO OUTPUT CLOCKING

Xylon's standard logiCVC-ML Compact Multilayer Video Controller IP core supports display resolutions up to 2048 x 2048. For information about support for higher display resolutions, please contact Xylon at info@logicbricks.com.

The logiREF-DISP-MicroZed reference design demonstrates the logiCVC-ML IP core implemented in Zynq-7000 AP SoC programmable logic. The logiCVC-ML display controller in this reference design drives Sharp's LCD (LQ070Y3LG4A) with 4-bit LVDS video interface. The display resolution is 800 x 480 pixels with pixel clock at 33.33 MHz, while the video timings are:

- vertical active lines: 480
- vertical front porch: 8
- vertical sync width: 2
- vertical back porch: 35
- horizontal active pixels: 800
- horizontal front porch: 40
- horizontal sync width: 128
- horizontal back porch: 88
- sync polarity: vsync active high, hsync inverted, data enable active high.

The logiCVC-ML internal structure is shown on the block diagram on Figure 5.1. The VCLK clock signal controls all circuits inside the logiCVC-ML IP core, except the video memory subsystem (PLB, XMB or AXI4) related circuits and registers (OPB, PLB or AXI4). The VCLK clock signal frequency should be set according to the display specifications.

Since the logiCVC-ML drives an LVDS video output, it requires its LVDS_CLK input to be driven with a clock that is 7xVCLK, which is 233.33 MHz. It is also important that VCLK and LVDS_CLK are synchronous.

LVDS video interface is comprised of a 4-bit differential data pair and a differential clock pair. The differential clock pair is synchronous to LVDS_CLK and has the same frequency.

LCD video timings, including sync polarity information are stored in corresponding logiCVC-ML registers. For more detailes please refer to the logiCVC-ML User's Manual document, Chapter 10.2. Register Description.

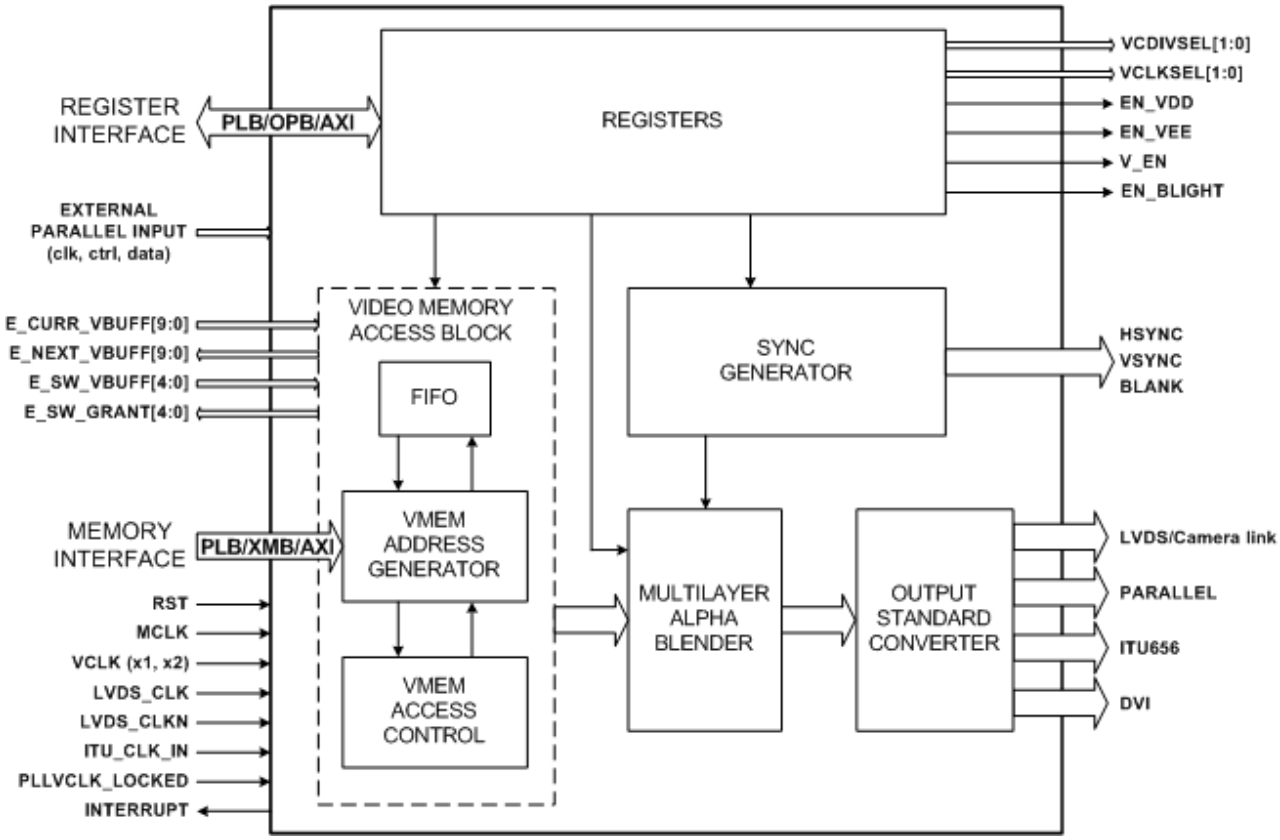


Figure 5.1 logiCVC-ML Architecture

5.1 Clock Module

A clock module is requested outside of the logiCVC-ML IP core to generate all the necessary clock for logiCVC-ML, as well as the PL to PS memory and register interface clock.

Xilinx Clocking Wizard is used in logiREF-DISP-MicroZed reference design to generate 3 clocks:

- clk_out1 – 100 MHz clock for PL to PS memory and register interface clock
- clk_out2 – 33.33 MHz clock for VCLK (LCDs pixel clock)
- clk_out3 – 233.33 MHz clock for LVDS_CLK (7xVCLK synchronous to VCLK)

Clocking Wizard has an input clock from the PS of 100 MHz. This clock is used for generating all output clocks.

6 QUICK START

6.1 Required Hardware

A full evaluation of the provided reference design requires:

- MicroZed Evaluation Kit (Part Number: AES-77MB-7Z010-G)
- I/O Carrier Card (Part Number: AES-MBCC-IO-G)
- 7-inch Zed Touch Display Kit (Part Number:AES-ALI2-ZED-G)
- SD card (min 512 MB)

- **optional**: USB cable, keyboard
- **optional**: USB Micro-B cable for debug UART
- **optional**: Ethernet cable for Telnet connection
- **optional**: Xilinx JTAG Platform cable for standalone application development

6.2 Xilinx Development Software

The logiREF-DISP-MicroZed reference design and Xylon logiCVC-ML IP core are fully compatible with Xilinx 2013.2 Vivado development tools. Future design releases shall be synchronized with the newest Xilinx development tools.

6.3 Set Up Linux System Software Development Tools

A set of ARM GNU tools is required to build the Linux software and applications. The complete tool chain for the Zynq-7000 All Programmable SoC can be obtained from the Xilinx ARM GNU Tools wiki page: http://wiki.xilinx.com/zynq-tools. Access to tools requires a valid, registered Xilinx user login name and password.

6.4 Set Up git Tools

Git is a free Source Code Management (SCM) tool for managing distributed version control and collaborative development of software. It provides the developer a local copy of the entire development project files and the very latest changes to the software.

Visit http://wiki.xilinx.com/using-git to get instructions how to use Xilinx git.

6.5 Set Up the MicroZed for Use with Precompiled Linux Demos from the SD Card

Xylon provides Linux and DirectFB demo binaries in the `ready_to_test` folder. If you want to run prepared demos, copy the content of the `ready_to_test` folder to the root folder on the FAT32 formatted SD card.

The logicBRICKS reference design utilizes touch controller for the demo applications, so there is no need for any keybord or mouse.

Avnet's ALI3 Sharp7 adapter is mounted on Sharp's LQ070Y3LG4A LCD. It contains LCD power control, PCAP touch controller and 4-bit LVDS video interface with DisplayPort connector.

Set up your MicroZed as shown on the Figure 6.1:

- set the jumpers identically to the settings shown on the figure
- connect keyboard to the OTG USB (connector J2), Ethernet cable (connector J2)
- plug in the SD card to card slot J6
- connect USB Micro-B cable for USB UART (connector J2)

Jumpers settings for the SD boot mode:

Jumper	Name	Setting
JT1	MODE0	LOW
JT2	MODE1	HIGH
JT3	MODE2	HIGH

Table 7.1 Jumpers Set Up for Booting from the SD Card

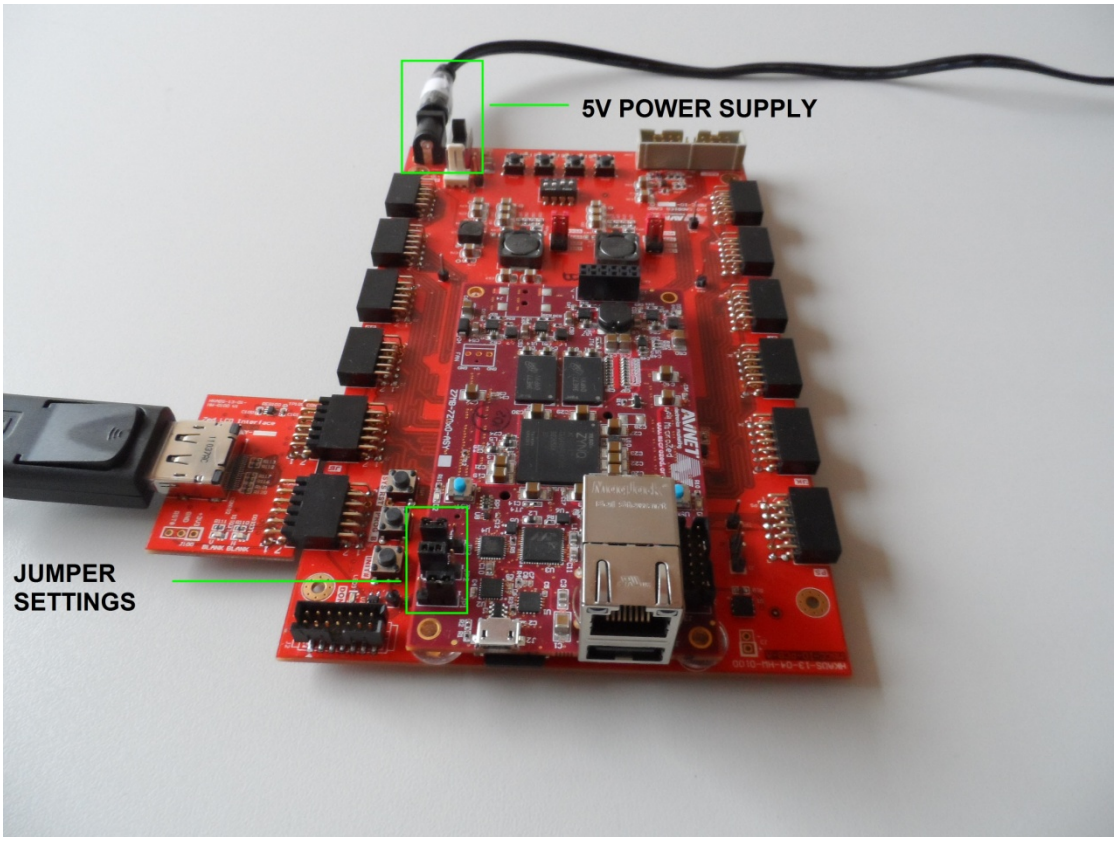


Figure 6.1 The MicroZed (Rev. B) Setup for the logicBRICKS Reference Design

MicroZed is powered through USB UART connection (J2). There is no additional power switch or connector on the board. Therefore, immediately upon plugging the cable, the board is powered up. The other way of powering the MicroZed is using the I/O carrier module card as shown on Figure 6.2. This module has an independent power connection (CON2) and switch (SW5). Both MicroZed and I/O carrier module require 5V powering.

For the logicBRICKS MicroZed reference design demos, the I/O carrier module is necessary because it is used to connect the LCD to MicroZed using PMOD-ALI3 module as shown on Figure 6.3. microheader connectors JX1 and JX2 on MicroZed are used to connect the I/O carrier module.

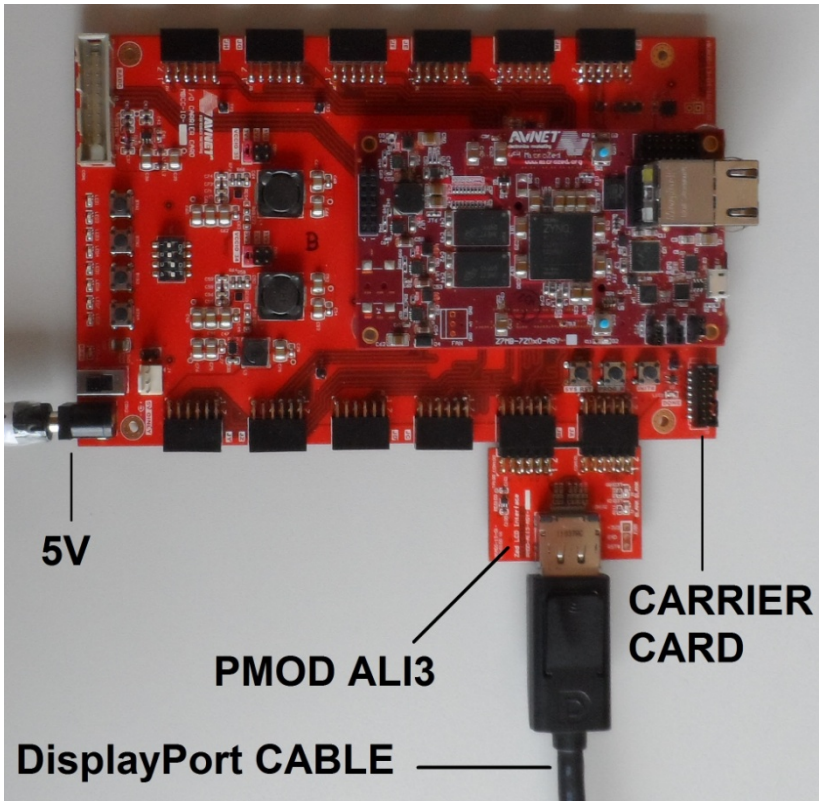


Figure 6.2 I/O Carrier Module and PMOD-ALI3

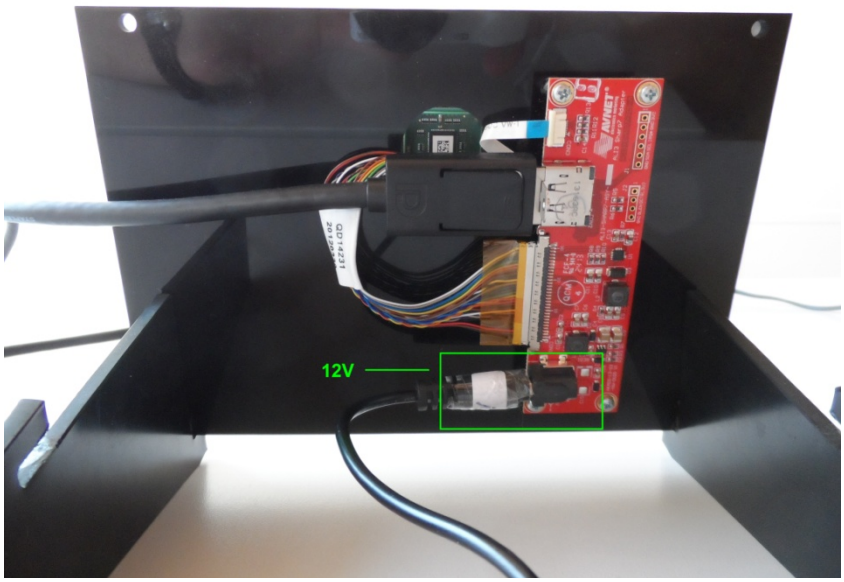


Figure 6.3 LCD Assembly

For full explanation of the MicroZed features and settings, please check the documentation provided with the kit.

6.6 Running Precompiled Demos from the SD Card Image

To quickly start precompiled Linux demos, make sure that you have the SD card with the precompiled image plugged in the board's slot, and all jumpers setup as described in the paragraph 6.5 Set Up the MicroZed for Use with Precompiled Linux Demos from the SD Card.

To control precompiled demos, you can:

- use the keyboard connected to the USB port and write commands directly to the screen console
- use serial terminal program (baud rate 115200) and USB UART connection to the MicroZed
- use telnet connection (IP address: 192.168.0.80) and Ethernet connection with the MicroZed

6.6.1 Running Demo Apps

There are two ways to run the demo applications; in which one system starts is determined by the value of `GUI_AUTOSTART` environment variable value in `init.sh` script on the SD card:

1. `GUI_AUTOSTART=true` – system boots automatically to ilixi application launcher (GUI),
2. `GUI_AUTOSTART=false` – system boots to command line and user should start the demos manually.

To start the demos manually type in the command line:

```
cd mnt
. vstartdfb.sh

# run some DirectFB demos ...
./df_texture  # control with the mouse, quit with 'q' not with CTRL-C
./df_knuckles # control with the mouse, quit with 'q' not with CTRL-C
./df_andi     # control with the keyboard, quit with 'q' not with CTRL-C
./df_dok      # quit with 'q' not with CTRL-C, observe CPU usage results!

# run some Ilixi demos ...
./ilixi_calc    # runs graphical calculator, CTRL-C to quit
./ilixi_carcomp # runs graphical application launcher, CTRL-C to quit

# run some Qt demos ...
./dials       # CTRL-C to quit
```

7 SOFTWARE DOCUMENTATION

Please use the `start.html` file (section 3.3. Directory Structure), or open directly `software/readme.html` file to find relevant documentation for building and using logiREF-DISP-MicroZed software deliverables. This file contains links to software documents and instructions related to Linux software.

7.1 Software Instructions – Linux Software

Xylon provides Linux frame buffer driver and DirectFB driver. Zynq toolchain, Linux kernel and file system used for development and demonstrations of Xylon drivers are provisions of Xilinx. Software provided comprises of:

- Xylon frame buffer driver for Linux kernel; Linux kernel building instructions, and DTS files
- Xylon DirectFB driver; general information and building instructions
- Ready to run Linux applications for the MicroZed Evaluation Kit on the prepared "ready_to_test" SD card image

8 REVISION HISTORY

Version	Date	Author	Approved by	Note
1.00.a	September 11, 2013	R. Končurat	G. Galić	Initial