logiREF-MULTICAM-ISP Multi-Camera HDR ISP Reference Design

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Figure 1: Parallel HDR ISP Processing of Four 2.3 MP Automotive Cameras by the Reference Design

Features

- The complete HDR ISP video processing framework for multi-camera embedded applications
- Demonstrates a logicBRICKS HDR ISP Pipeline for parallel processing of four automotive video cameras
- Optimized for Xilinx® programmable FPGA/SoC/MPSoC/ACAP devices
- Jump-starts development and saves valuable design time
- Fully compatible with Xylon's logiISP-ZU-GMSL2 Evaluation Kit based on the Xilinx® Zynq® UltraScale+™ MPSoC
- The design is prepared for the Xilinx Vivado® Design Suite 2020.2
- Runs on Linux OS and includes logicBRICKS software drivers and demo applications made with the Xilinx Vitis™ Unified Software Platform 2020.2
- Design demonstrates programmable logic savings achieved by multiplexing of ISP functions
- Includes licensed[1] Xylon logicBRICKS IP cores
- Resolutions: IN 1928x1208 and OUT 1920x1080
- HDMI™ display output with the Xilinx HDMI 1.4/2.0 Transmitter Subsystem[2] controlled via Xylon's DRM kernel driver
- Documentation and Tech support (e-mail)

1. *Included 3-month Xylon seat evaluation licenses for used Xylon logicBRICKS IP cores.*
2. *Xilinx licensed IP. Digital code vouchers provided by Xylon to buyers of the logiISP-ZU-GMSL2 HDR ISP Evaluation Kit.*

Applications

- AD/ADAS, AI, guided robotics, drones, machine vision, AR/VR and other vision applications

General Description

Xylon offers a complete logicBRICKS IP suite for implementing High-Dynamic Range (HDR) Image Signal Processing (ISP) pipelines in embedded designs based on Xilinx FPGA, SoC, MPSoC or ACAP programmable devices. HDR ISP pipelines enable crisp camera video under altering and rough lighting conditions in next-generation multi-channel embedded systems for use in automotive, surveillance, medical and similar video and vision AI applications.

logicBRICKS ISP IP cores enable parallel processing of multiple Ultra HD video inputs in different Xilinx devices, ranging from the small Xilinx Artix® FPGAs to the latest Xilinx Versal™ Adaptive Compute Acceleration Platform (ACAP) devices.
The logiREF-MULTICAM-ISP demonstrates these capabilities and shows how, in comparison to simple instantiation of multiple ISP pipelines within a single programmable device, Xylon's logicBRICKS ISP pipeline allows for tremendous savings of up to 50 % of valuable programmable logic.

Key IP cores, the logiISP-UHD ISP pipeline and the logiHDR HDR pipeline, support parallel processing of multiple video inputs, resolutions up to 7680x7680 (including the popular 4K2Kp60 video resolution), merging of two or three exposures, parallel pixel processing and different pixel formats. These IP cores for programmable logic implementations are supplemented with AWB and AE software libraries that use video statistics data collected at the video inputs, software drivers, demo applications, reference SoC designs, and bit-accurate C-models.

The logiREF-MULTICAM-ISP reference design can be fully evaluated on the logiISP-ZU-GMSL2 hardware platform designed by Xylon. This platform is based on the Xilinx Zynq® UltraScale+™ MPSoC and includes four of Xylon's 2.3 MP HDR logiCAM-GMSL2 automotive cameras configured to output raw Bayer video.

If you are interested in Xilinx Versal ACAP implementations of the logicBRICKS HDR ISP pipelines, please contact Xylon at info@logicbricks.com or visit our website www.logicbricks.com to learn more about our current offerings.

Example Implementation Statistics

Table 1 shows programmable logic savings achieved by the multi-channel logiREF-MULTICAM-ISP reference design in comparison to a simple instantiation of four parallel and equivalent ISP pipelines. Of course, this example relates to a specific set of ISP features, camera type, resolution, etc. The level of programmable logic savings depends on the specific implementation case.

Table 1: Programmable Logic Savings Achieved by the Multi-Cam Parallel ISP Processing

	Saved resources (4xOneCAM – MULTICAM)	Used resources	
		logiREF-MULTICAM-ISP	4xOneCAM
Look-Up Tables (LUTs)	24748	25864	50612
Flip Flops (FFs)	36438	31302	67740
LUTRAMs	5271	2901	8172
Block RAM (36 kB BRAM)	12	118	130
DSP slices (MULT/DSP)	288	116	404

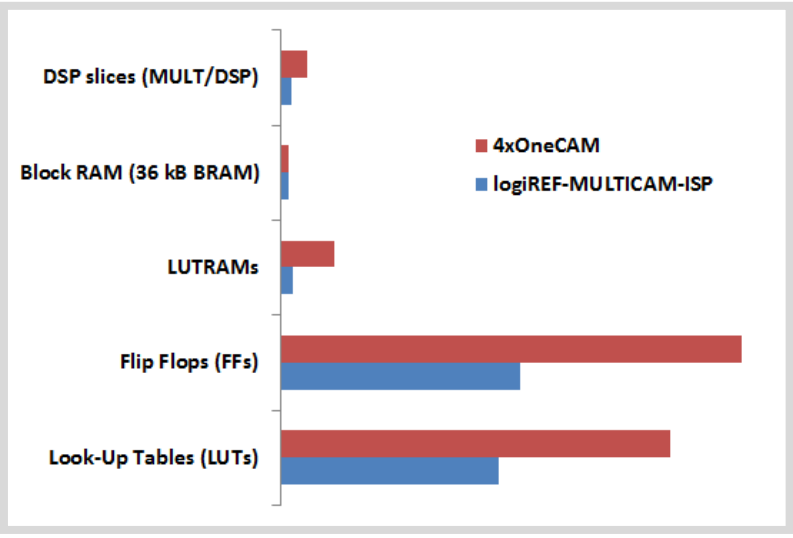

Figure 2: Comparison of Used Programmable Logic Resources for Four Camera HDR ISP Processing

logiREF-MULTICAM-ISP Reference Design

This MPSoC design supports four camera inputs multiplexed and processed by one ISP pipeline. The following figure shows the ISP subsystem. Xylon's logiFMC-GMSL2 FMC module sends three MIPI CSI-2 streams towards the Xilinx MPSoC device. One of the MIPI streams is actually operating in the MIPI aggregate mode and contains video data from two cameras. Video streams are distinguished by different MIPI virtual channels (VC).

The block diagram shows that the provided IP blocks can be arranged in many different ways to fully tune up the system for a specific application. While hardware engineers may configure and arrange IP blocks implemented in programmable logic in various ways, software engineers can further control the implemented ISP pipeline to adapt to changing use conditions.

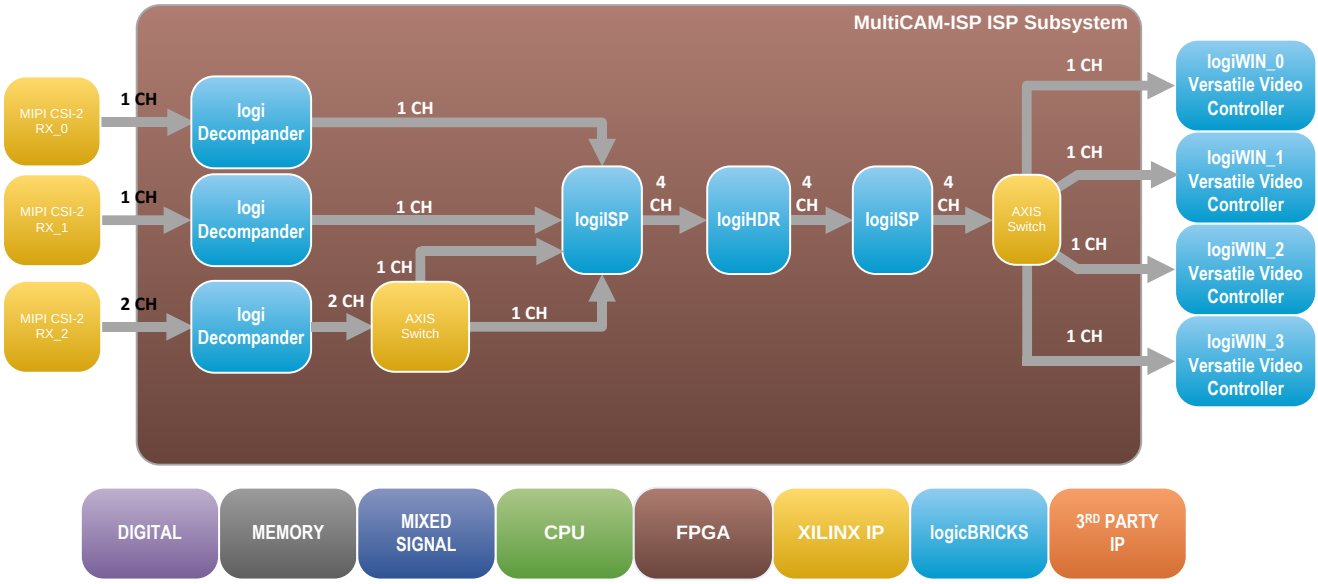

Figure 3: ISP Subsystem Block Diagram

Reference Design Content

Hardware Design Files[1]

- Hardware description file (HDF) for Vitis export of the reference design that allows for instant design check-up and software changes
- Reference design prepared for the Xilinx Vivado Design Suite (script-based)
- Xylon's evaluation logicBRICKS IP cores:
  - logiCVC-ML Compact Multilayer Video Controller
  - logiWIN Versatile Video Input
  - logiISP-UHD Image Signal Processing (ISP) Ultra HD Pipeline
  - logiHDR High Dynamic Range (HDR) Pipeline
  - Xylon Utility IP cores

Software[1]

- Petalinux 2020.2 build BSP
- Linux user space drivers with driver examples
- Linux user space software libraries
- Bare-metal software drivers with driver examples for logicBRICKS IP cores
- Bare-metal software librariers
- Platform software libraries
- Demo application sources

[1] *Included 3-month Xylon seat evaluation licenses for used Xylon logicBRICKS IP cores.*

Binaries

- Configuration bitstream (FPGA/PL)
- Precompiled AWB and AE software libraries
- Linux binaries:
  - boot.bin
    - First Stage Boot Loader (FSBL)
    - Bitstream
    - Second Stage Boot Loader (SSBL – U-boot)
    - Platform Management Unit Firmware and ARM trusted software
  - image.ub
    - kernel image
    - device tree blob
    - minimal Root File System
  - Custom start (init.sh)
  - logiREF-MULTICAM-ISP demo Linux application executables
- Standalone binaries (MULTICAM-ISP demo standalone application executables)

Evaluation Kit

The licensed logiREF-MULTICAM-ISP reference design is delivered as part of the complete logiISP-ZU-GMSL2 Evaluation Kit. This HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and develop multi-camera vision applications on Xilinx's Zynq UltraScale+ MPSoC devices. The complete hardware platform includes four of Xylon's 2.3 MP automotive video cameras with the raw Bayer video output and supports the HDMI video output.

To learn more about it, please visit: https://www.logicbricks.com/Solutions/Xylon-HDR-ISP-Pipeline.aspx

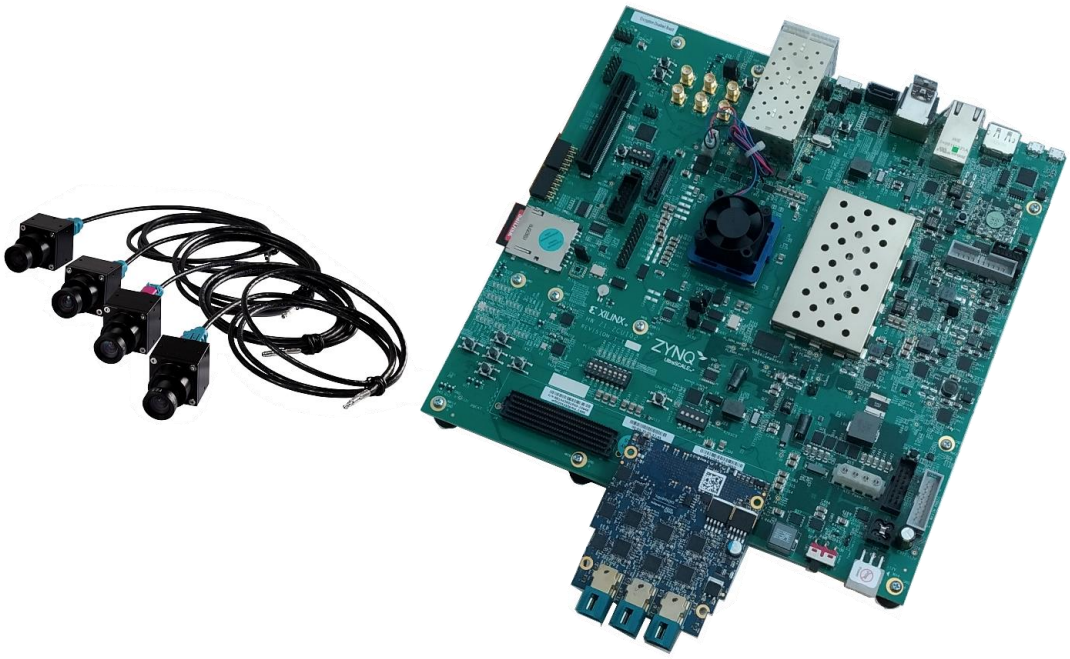

Figure 4: logiISP-ZU-GMSL2 Evaluation Kit

Recommended Design Experience

Users that want to make changes on the provided designs should have experience in the following areas:

- Xilinx design tools
- C programming
- Embedded hardware and software design

All logicBRICKS IP cores provided with the design framework are fully compatible with Xilinx's implementation tools and their use does not require any particular skillset beyond general Xilinx tools knowledge.

Related Xylon Products

The logiISP-ZU-GMSL2 HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to efficiently develop multi-camera vision applications on Xilinx's Zynq UltraScale+ MPSoC devices.The complete hardware platform includes four of Xylon's 2.3MP automotive video cameras with the raw Bayer video output and supports the HDMI video output to control a monitor.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiISP-ZU-GMSL2.aspx

The ISP-UHD is an Ultra High Definition (UHD) ISP pipeline designed for digital processing and image quality enhancements of raw image data from video sensors. The logiISP-UHD accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data, manipulated video data formats and color domains…:

URL: https://www.logicbricks.com/Products/logiISP.aspx

The logiHDR is an Ultra High Definition (UHD) HDR pipeline designed for digital processing and image quality enhancements of raw image data from HDR sensors. The logiHDR extracts maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by direct sunlight and objects placed in extreme shades:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHDR.aspx

Xylon provides software Auto White Balance (AWB) and Auto Exposure (AE) libraries for use with the logiISP-UHD IP core. To get more information about these products, please contact Xylon:

Email: info@logicbricks.com

Ordering Information

Products are available directly from Xylon. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00	17.05.2021.	Initial public release.
2.00	16.09.2021.	Updated Table 1. Updated Figure 4. Avnet HDMI FMC replaced with native board's connector and Xilinx HDMI TX IP Core Subsystem.

