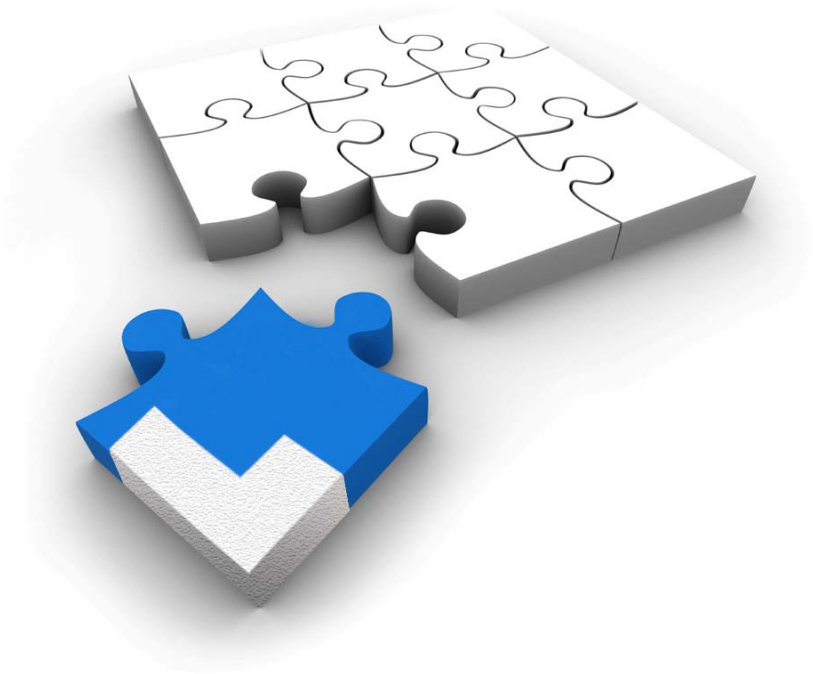
logiREF-ZHMI-FMC

Xylon Reference Design – Human-Machine Interface for Xilinx® Zynq™-7000 All Programmable SoC

User's Manual

Version: 1.01.a

logiREF-ZHMI-FMC_v1_01_a.doc



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1 INTRODUCTION

Xylon's logicBRICKS IP Cores provides an easy plug-and-play experience and enable fast development of customized Human Machine Interfaces (HMI) for Xilinx® Zynq™-7000 and FPGA programmable devices.

This user's manual describes Xylon's HMI reference design for the ZC702 The reference design includes evaluation logicBRICKS IP cores and hardware design files prepared for Xilinx Platform Studio (XPS) design suite. It also includes complete Linux OS image, software drivers, demo applications and documentation for video image capture, touch digitizer control, audio, 2D/3D graphics and display control.

System designers can leverage the flexibility and scalability of logicBRICKS IP cores and software to speed up their development cycle. Software designers can develop Linux and standalone applications for their product before target hardware is available and hardware designers can customize the provided logicBRICKS designs to closely fit to their requirements.

logicBRICKS IP cores can be delivered with software drivers for the most popular operating systems: Linux, Microsoft® Windows® Embedded Compact 7 and Android™.

Figure 1: Xilinx ZC702 Development Kit running live video stream from camera

(Video clip: http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Demos-Xilinx-ZC702-Video-Clip.aspx)

The design is prepared for the Xilinx® Platform Studio (XPS) and the EDK implementation tools. It is a comprehensive HMI comprised of a set of logicBRICKS evaluation IP cores, the full FPGA design, documentation and a number of illustrative software applications demonstrating specific IPs' features.

The logicBRICKS reference design helps users to experience the logicBRICKS design flow at no cost and with no obligations! The provided software exercises logicBRICKS IP drivers and illustrate the most important IP features.

1.1.1 Hardware design files

- Configuration bitstream file for the programmable logic and the SDK export of the reference design that allow an immediate start and software changes
- ZC702 reference design[1] prepared for Xilinx Platform Studio implementation tools
- Xylon evaluation logicBRICKS IP cores[1]:
    - logiCVC-ML Compact Multilayer Video Controller
    - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
    - logiBMP Bitmap 2.5D Graphics Accelerator
    - logi3D Scalable 3D Graphics Accelerator
    - logiWIN Versatile Video Input
    - logiI2S I2S Multiport Controller

1.1.2 Software

- logicBRICKS standalone (bare-metal drivers) with driver examples
- Zynq FSBL sources and the Xilinx SDK project - custom version for standalone applications
- Linux Frame Buffer driver for the logiCVC-ML IP core (display controller IP Core)
- DirectFB driver for logiCVC and 2D hardware acceleration (logiBITBLT)
- logi3D example sources and binaries (OpenGL ES 1.1[2] library for logi3D IP is provided on request)

1.1.3 Binaries

- First Stage Bootloader (FSBL)
- standalone logiCVC-ML, logiBITBLT examples
- standalone fmc_test program
- Linux binaries:
    - uboot, dts, dtb, root file system
    - zImage - kernel with the frame buffer driver for the logiCVC-ML IP Core
    - DirectFB library and DirectFB examples using Xylon DirectFB driver
    - OpenGL ES 1.1 simple example and Xylon 3D demo

1.2 Xilinx Development Software

The logiREF-ZHMI-FMC reference design and Xylon logicBRICKS™ IP cores are fully compatible with Xilinx development tools – Xilinx Design Suite 14.2 including Xilinx ISE, Xilinx Platform Studio (XPS) and the EDK. Future design releases shall be synchronized with the newest Xilinx development tools.

Licensed users of the Xilinx tools can use their existing software installation for the logiREF-ZHMI-FMC evaluation. Suitable ISE Design Suite versions are: Embedded and System Edition.

[1] Delivery is optional
[2] Product is based on a published Khronos specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

Others may use ISE® Design: Suite Embedded Edition from Evaluation Kit or download evaluation versions of Xilinx software development tools from the Xilinx Web site (www.xilinx.com).

2 LOGICBRICKS IP CORES

2.1 About logicBRICKS IP Library

Xylon's logicBRICKS IP core library provides IP cores optimized for Xilinx FPGA and Zynq-7000 All Programmable SoC. logicBRICKS IP cores shorten development time and enable fast design of complex embedded systems based on Xilinx programmable devices.

The key features of the logicBRICKS IP cores are:

- Compatibility with the Xilinx Platform Studio (XPS) – logicBRICKS can be used in a same way as Xilinx IP cores from the XPS, and require no skills beyond general tools knowledge
- Each logicBRICKS IP core comes with the extensive documentation, reference design examples and can be evaluated on reference hardware platforms
- Broad software support – from bare-metal software drivers to standard software drivers for different operating systems (OS). Standard software support allows graphics designers and software developers to use logicBRICKS in a familiar and comfortable way
- Xylon assures skilled technical support

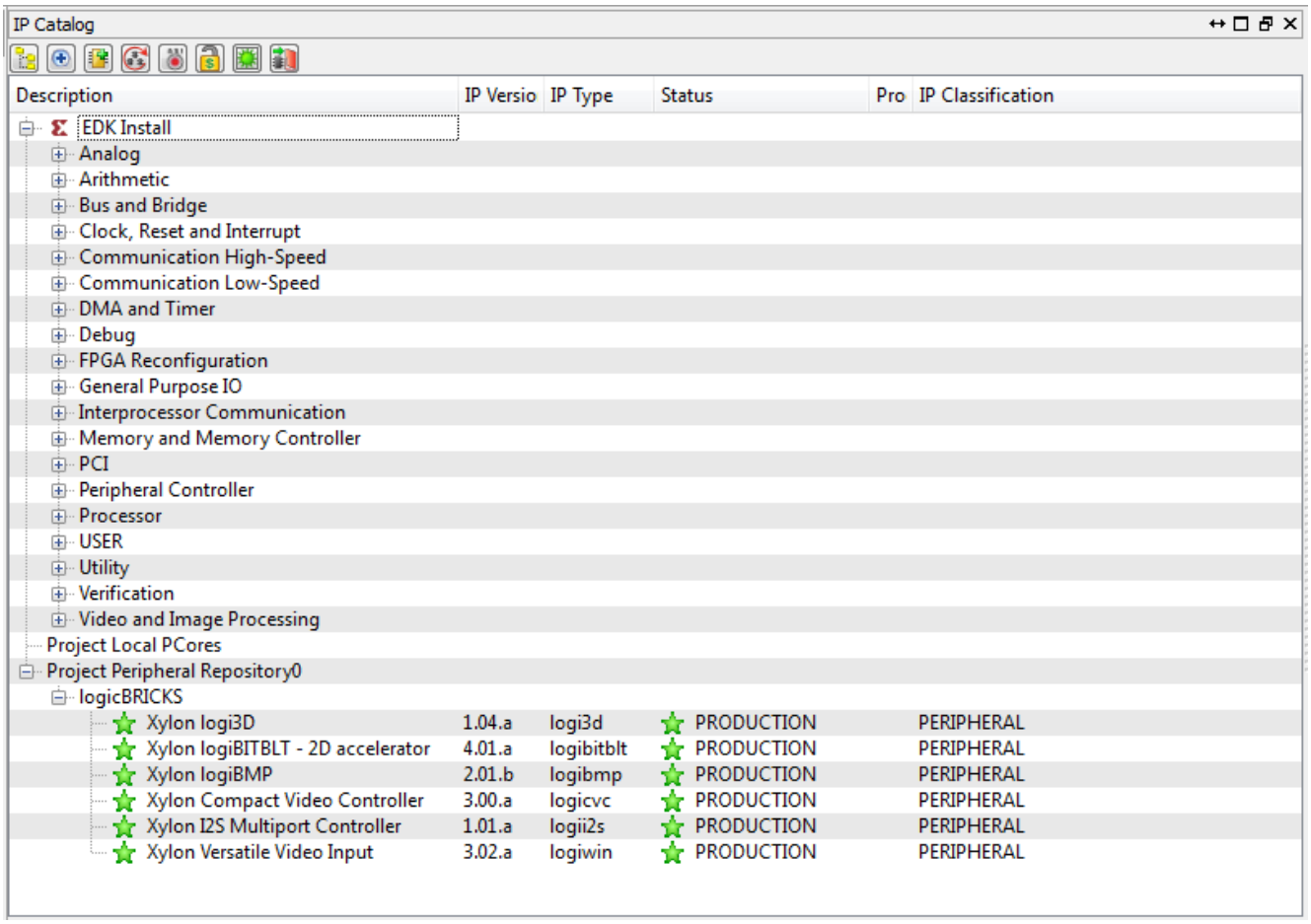


Figure 2: logicBRICKS IP Cores Imported into the XPS IP Catalog

The Figure 2 shows imported logicBRICKS IP cores into Xilinx development software, while the Figure 3 shows a typical logicBRICKS IP core's configuration GUI.

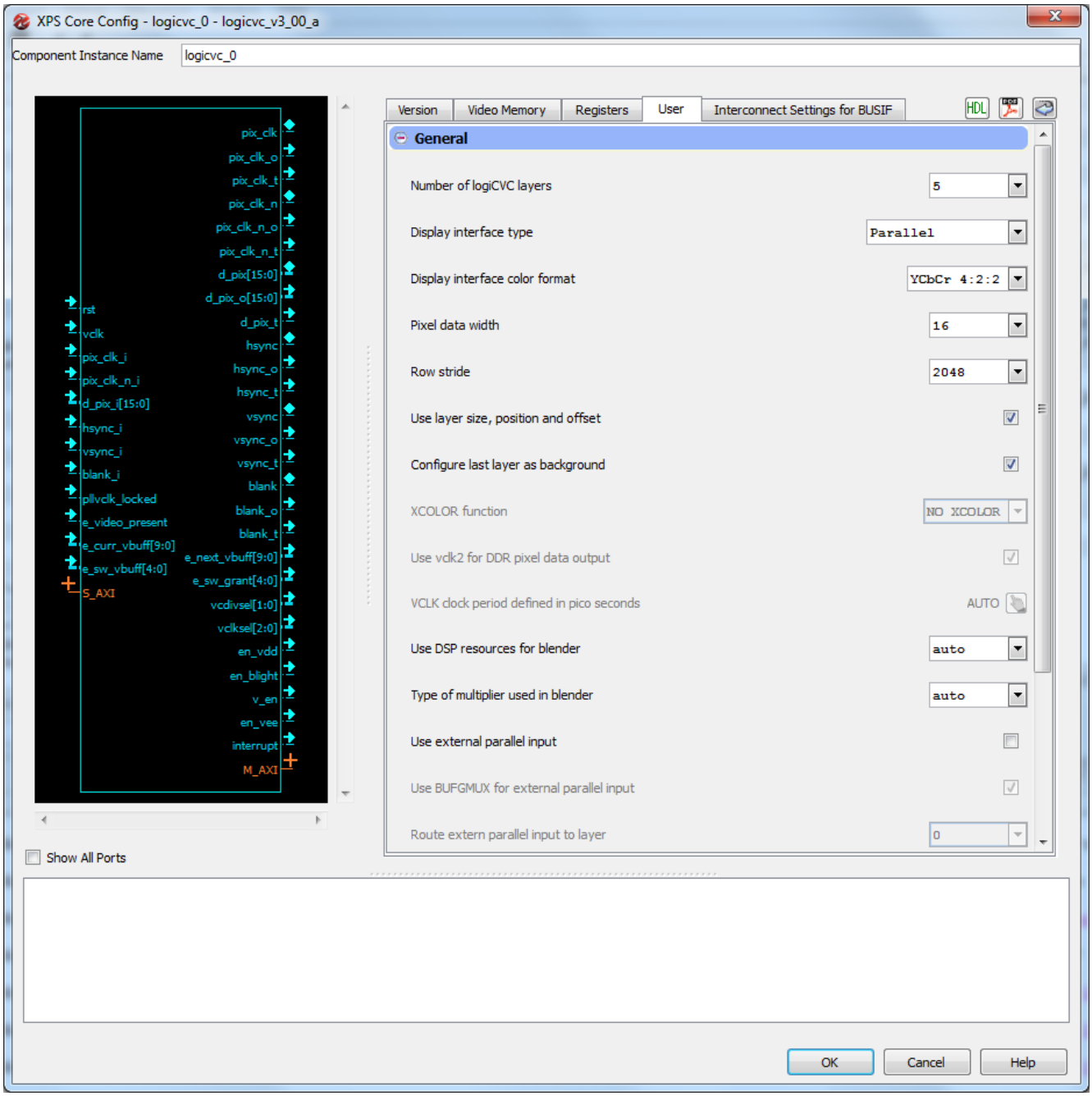


Figure 3: An Example logicBRICKS IP Configuration GUI

Click on the PDF icon in the GUI opens the User's Manual of the logicBRICKS IP Core!

2.2 Evaluation logicBRICKS IP Cores

Xylon offers free evaluation logicBRICKS IP cores which enable full hardware evaluation:

- Import into the Xilinx Platform Studio (XPS)
- IP parameterization through the XPS GUI interface
- Simulation (if Xilinx tools support it)
- Bitstream generation

The logicBRICKS evaluation IP cores are run-time limited and cease to function after some time. Proper operation can be restored by reloading the bitstream. Besides this run-time limitation, there are no other functional differences between the evaluation and fully licensed logicBRICKS IP cores.

Evaluation logicBRICKS IP cores are distributed as parts of the Xylon reference designs: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx.

Specific IP cores can be downloaded from Xylon's web shop: http://www.logicbricks.com/Products/IP-Cores.aspx.

2.3 logicBRICKS IP Cores Used in This Design

2.3.1 logiCVC-ML Compact Multilayer Video Controller

The logiCVC-ML IP core is an advanced display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems with Xilinx Zynq-7000 All Programmable SoC and FPGAs.

This IP core is the cornerstone of all 2D and 3D GPUs. Though its main function is to provide flexible display control, it also includes a level of hardware acceleration: alpha blendings, panning, buffering of multiple frames, etc.

- Supports all Xilinx FPGA families
- Supports LCD and CRT displays (easily tailored for special display types)
- 64x1 to 2048x2048 display resolutions
- Support for higher display resolutions available on request
- Supports up to 5 layers; the last one configurable as a background layer
- Configurable layers' size, position and offset
- Alpha blending and Color keyed transparency
- Pixel, layer, or color lookup table (CLUT) alpha blending mode can be independently set for each layer
- Packed pixel layer memory organization – pixel color depth 8-bpp, 8-bpp using CLUT, 16bpp Hi-color RGB 565 and True-Color 24bpp
- Configurable CoreConnect™ PLBv4.6, Xylon XMB or ARM® AMBA® AXI4 memory interface data width (32, 64 or 128)

- Programmable layer memory base address and stride
- Simple programming due to small number of control registers
- Support for multiple output formats:
  - Parallel display data bus: 12x2-bit, 15-bit, 16-bit, 18-bit or 24-bit
  - Digital Video ITU-656: PAL and NTSC
  - LVDS output format: 3 or 4 data pairs plus clock
  - Camera link output format: 4 data pairs plus clock
  - DVI output format
  - YCbCr 4:4:4 or 4:2:2 output format
- Supports synchronization to external parallel input
- HW cursors
- Versatile and programmable sync signals timing
- Double/triple buffering enables flicker-free reproduction
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK

More info: http://www.logicbricks.com/Products/logiCVC-ML.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCVC-ML_hds.pdf

2.3.2 logiBITBLT Block Transfer 2D Graphics Accelerator

The logiBITBLT 2D graphics accelerator IP core transfers graphics objects from one to another part of system's on-screen or off-screen video memory, and off-loads the processor.

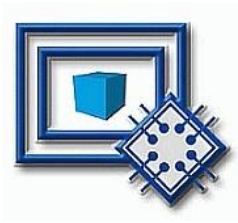
The core also performs different operations during transfers, such as ROP2, Color Expansion, Transparency, and Porter & Duff compositing rules. The IP can be efficiently used for the most common GUI operations.

- Supports 16 different ROP2 Binary Raster Operations
- Porter-Duff image composition with/without the global alpha blending factor
- Contiguous and array image addressing modes
- Color-keyed transparency
- Anti-aliased 8-bit font expansion
- Pattern fill with 8x8 pixels patterns
- Supports move operations in positive direction without image artifacts caused by image overlapping
- Solid fill with any of the supported color formats
- Supported image formats: RGB8, ARGB8, RGB16, ARGB16, RGB24, and ARGB24
- Control of pixel alpha blending factors
- Register interface compatible to the AXI4-Lite bus
- Designed for interfacing AXI4 master memory interface. Other memory interfaces can be supported on request
- Memory and registers layout both configurable for big and little endianness
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings

- Prepared for Xilinx Platform Studio (XPS) and the EDK

More info: http://www.logicbricks.com/Products/logiBITBLT.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiBITBLT_hds.pdf

2.3.3 logi3D Scalable 3D Graphic Accelerator



The logi3D Scalable 3D Graphics Accelerator IP core is a 3D Graphics Processing Unit (GPU) IP core developed for embedded systems based on the Xilinx Zynq-7000 All Programmable SoC.

The IP is designed to support the OpenGL ES 1.1 API specifications - a royalty-free, cross-platform API for full-function 2D and 3D graphics on embedded systems - including consoles, phones, appliances and vehicles.

- Graphics Accelerator IP designed to support the OpenGL® ES 1.1 API (Common Profile)
- Conformant to the AMBA® AXI4 bus specifications from ARM®
- Compatible with popular operating systems
- FPGA resource-effective 3D acceleration
- ARM Cortex™ -A9 CPU Core with NEON™ runs the geometry engine and optimizes the IP's size
- The logi3D can be used with different CPUs
- Hardware implemented 3D graphics algorithms:
    - Occlusion culling
    - Gouraud shading
    - MIP-MAP level of the texture per pixel
    - Texture filtering: point sampling, bilinear filtering and trilinear filtering
    - Fog function per vertex
    - Alpha Blending
    - Full Screen Antialiasing
- Parametrical VHDL design that allows tuning of slice consumption and features set

More info: http://www.logicbricks.com/Products/logi3D.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logi3D_hds.pdf

2.3.4 logiI2S Audio Data Receiver/Transmitter

The logiI2S is an audio receiver and transmitter IP core from the Xylon logicBRICKSTM IP core library. It is designed to transport stereo audio data between processors and codecs. The logiI2S supports a configurable amount of I2S transmitters and receivers, up to a maximum of 4 transmitters and 4 receivers. Each individual transmitter and receiver can be configured as either clock master or slave.

- Supports Xilinx® Zynq™-7000 AP SoC and all FPGAs
- Configurable number of I2S transmitters and receivers, up to 4 transmitters and 4 receivers

- Each transmitter/receiver can be configured as either clock master or slave
- Each transmitter/receiver can be configured as either word select master or slave
- Supports three different justification modes
- TX/RX FIFOs depth selectable from 512 up to 2048 words
- Supported word lengths up to 16 bits
- ARM® AMBA® AXI4-Lite bus compliant
- Fully embedded into Xilinx XPS and the EDK

More info: http://www.logicbricks.com/Products/logiI2S.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiI2S_hds.pdf

2.3.5 logiWIN Versatile Video Input

The logiWIN IP core accepts a streaming video input, decodes it and converts into the RGB format. The input video can be real-time scaled, de-interlaced, cropped and positioned on the video display. Captured and processed video must be displayed by a graphics controller IP, i.e. the Xylon logiCVC-ML Compact Multilayer Video Controller. The logiWIN integrates high-quality anti-aliasing algorithm that guarantees high picture quality without visible artifacts.

- Supports Xilinx® Zynq-7000 EPP and FPGAs
- Maximum input and output resolutions 2048x2048
- Supports ITU656 or ITU1120 (PAL, NTSC) and RGB inputs
- Real-time scale-up to 64x and scale-down to 16x
- Supports video de-interlacing, cropping, positioning
- Supports pixel alpha blending
- Embedded image color enhancements: brightness, contrast, hue, saturation
- Configurable register interface: AMBA® AXI4-Lite, CoreConnect™ OPB or PLB
- Configurable video memory interface: AMBA AXI4, Xylon XMB, PLB or Xilinx MPMC
- Fully embedded into Xilinx XPS and EDK

More info: http://www.logicbricks.com/Products/logiWIN.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiWIN_hds.pdf

2.4 logicBRICKS IP Cores for Video Processing

Xylon offers several logicBRICKS IP cores for video processing on Xilinx Zynq-7000 All Programmable SoC and FPGA programmable devices, which can be used as extensions to Xylon 2D and 3D graphics engines, or as key IP cores for video-only embedded applications.

All logicBRICKS IP cores support ARM AMBA AXI4 on-chip bus and can be easily mixed together, or with Xilinx and third-party IP cores.

Removes fish-eye lens distortions and executes programmable transformations on multiple video inputs in a real time. Programmable homographic transformation enable: cropping, resizing, rotating, transiting and arbitrary combinations. Arbitrary non-homographic transformations are supported by programmable Memory Look-Up Tables (MLUT).

More info: http://www.logicbricks.com/Products/logiVIEW.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiVIEW_hds.pdf

Converts Bayer color coded video inputs into RGB video. Supports all possible Bayer patterns. Supports input resolutions up to 2048x2048. Also supports input video scaling.

More info: http://www.logicbricks.com/Products/logiBAYER.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiBAYER_hds.pdf

3 GET AND INSTALL THE REFERENCE DESIGN

Xylon offers several logicBRICKS reference designs for different hardware platforms. Short descriptions of all Xylon logicBRICKS reference designs can be found at:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

A quick access to specific reference design is also possible through the main downloads navigation page: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

Only registered logicBRICKS users can download logicBRICKS reference designs. Unregistered users will be re-directed to the User Login page. The download link is automatically sent by an e-mail, which means that the registration process requires an access to the e-mail account.

Xylon reference logicBRICKS designs can be downloaded as self-extracting installers compatible with Microsoft Windows operating systems, or as a cross-platform Java JAR self-extracting installer.

3.1 Registration Process

Registration is very quick and simple. If you experience any troubles during the registration process, please contact Xylon Technical Support Service – support@logicbricks.com.

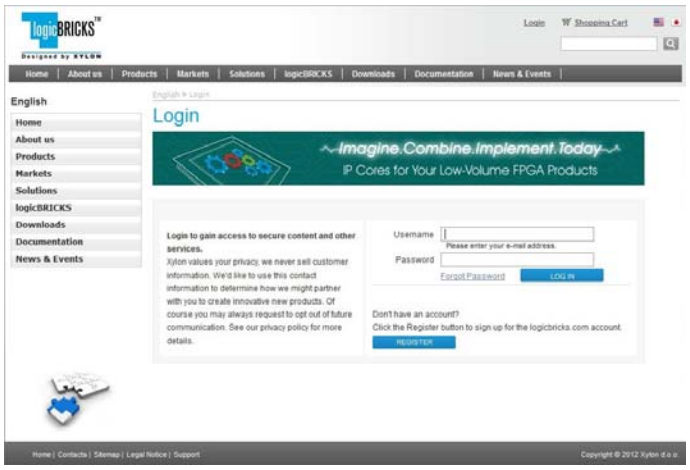


Figure 4: Registration Process – Step 1

Step 1

If you are the registered logicBRICKS user, please type-in your Username and Password. Unregistered users should click on the Register button, which will open the registration form.

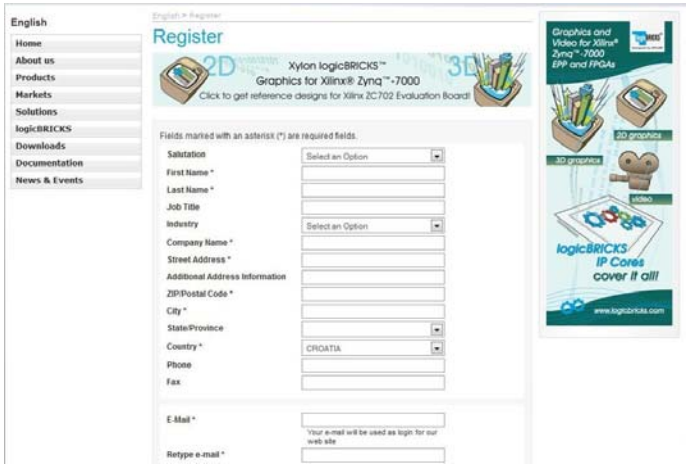


Figure 5: Registration Process – Step 2

Step 2

Unregistered users should fill-in the registration form from the Figure 5. Please take care on required form's fields. Your Username is an actual e-mail account used for communication with Xylon logicBRICKS. Xylon accepts only valid company e-mail accounts.

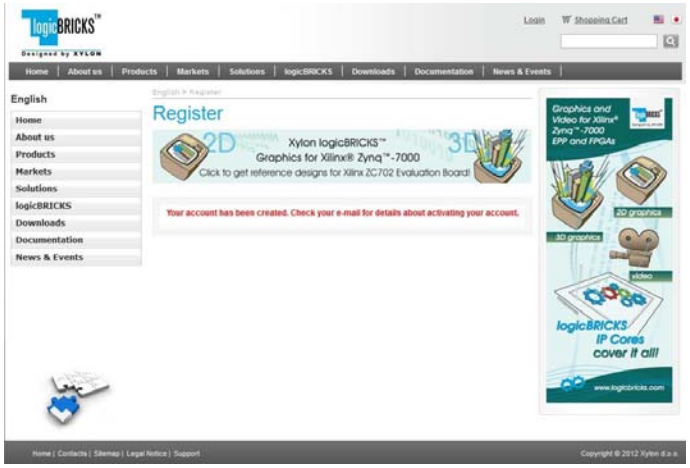


Figure 6: Registration Process – Step 3

Step 3

As soon as your registration form gets accepted by Xylon, you get a confirmation message. Please check your e-mail to find a link that activates your logicBRICKS account. If you do not get the confirmation message in several minutes, please contact Xylon support.

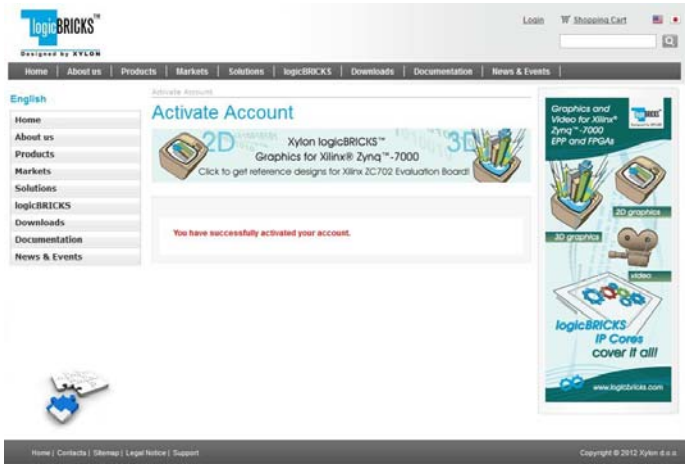


Figure 7: Registration Process – Step 4

Step 4

Click on the logicBRICKS web account activation link in the received e-mail, and you will get the confirmation status message. Please login to proceed.

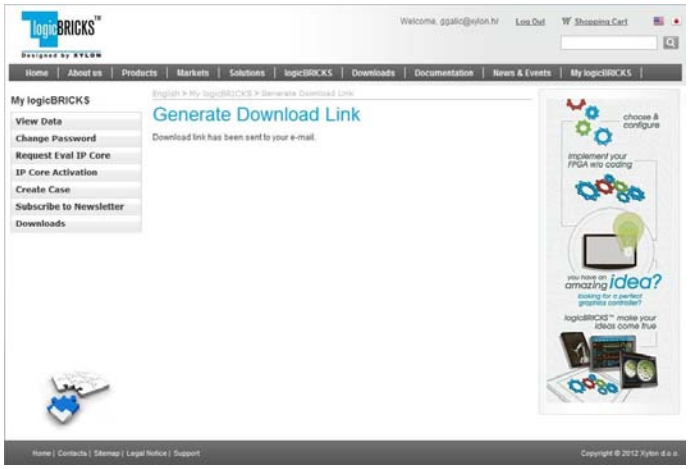


Figure 8: Registration Process – Step 5

Step 5

As soon as you select an appropriate logicBRICKS reference design and installer for your operating system from the Downloads Navigation Page (link bellow), you will get an e-mail with the download link for the selected reference design installation.

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

3.2 Installation Process

Installation process is quick and easy. Start the self-extracting installer (JAR or EXE). At the beginning, you will be requested to accept two evaluation licenses – Figure 22 and Figure 10.

For installation in Linux OS, please follow instructions: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Linux-Installation.aspx.

If you agree with the conditions from the evaluation licenses, click NEXT and select the installation path for your logicBRICKS reference design – Figure 11.

The installation process takes several minutes. It generates the directory structure described in the chapter 3.3 Directory Structure.

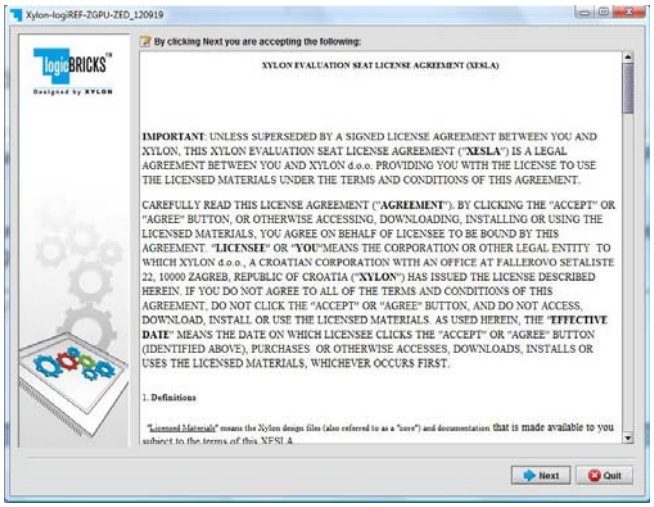


Figure 9: Installation Process – Step 1

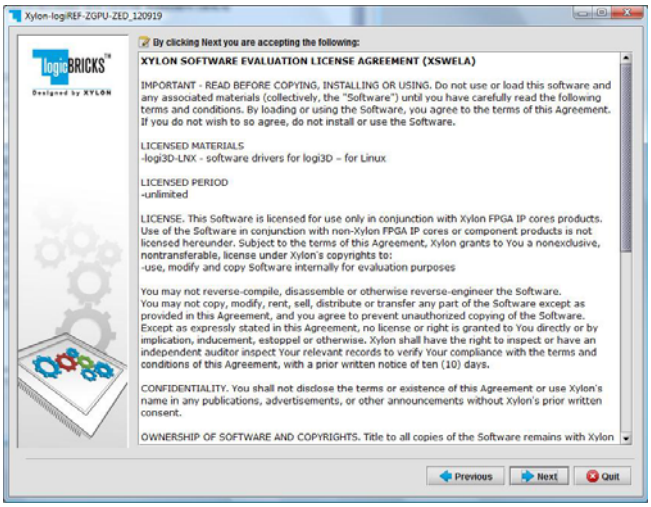


Figure 10: Installation Process – Step 2

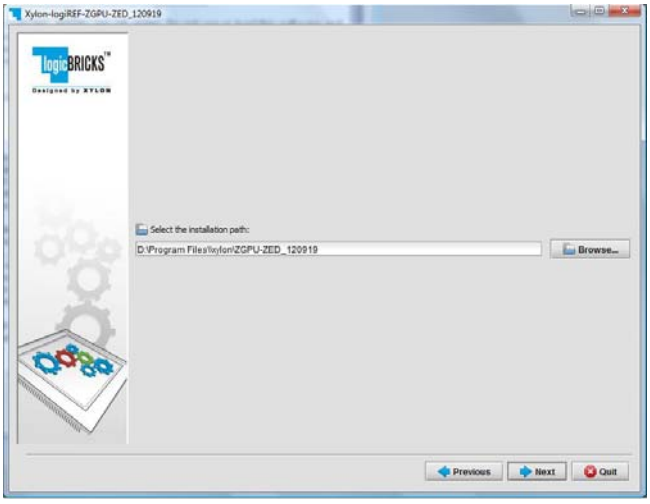


Figure 11: Installation Process – Step 3

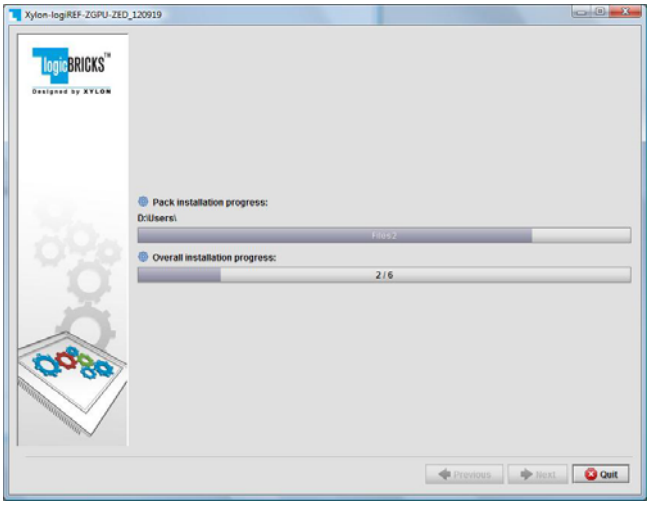


Figure 12: Installation Process – Step 4

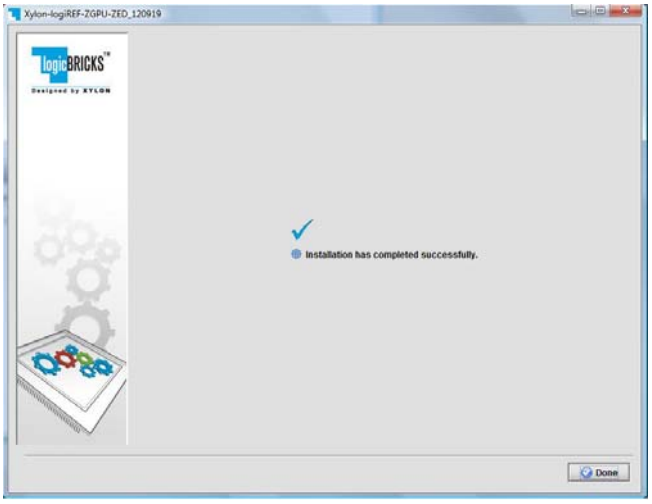


Figure 13: Installation Process – Step 5

3.3 Directory Structure

Figure 14 gives a top level view of the directories and files included with the logiREF-ZHMI-FMC reference design for the ZC702 Board development kit. Table 1 provides quick explanations of directories' purpose.

Please use the `start.html` file located in the installation root directory as a jump-start navigation page for exploring the reference design.

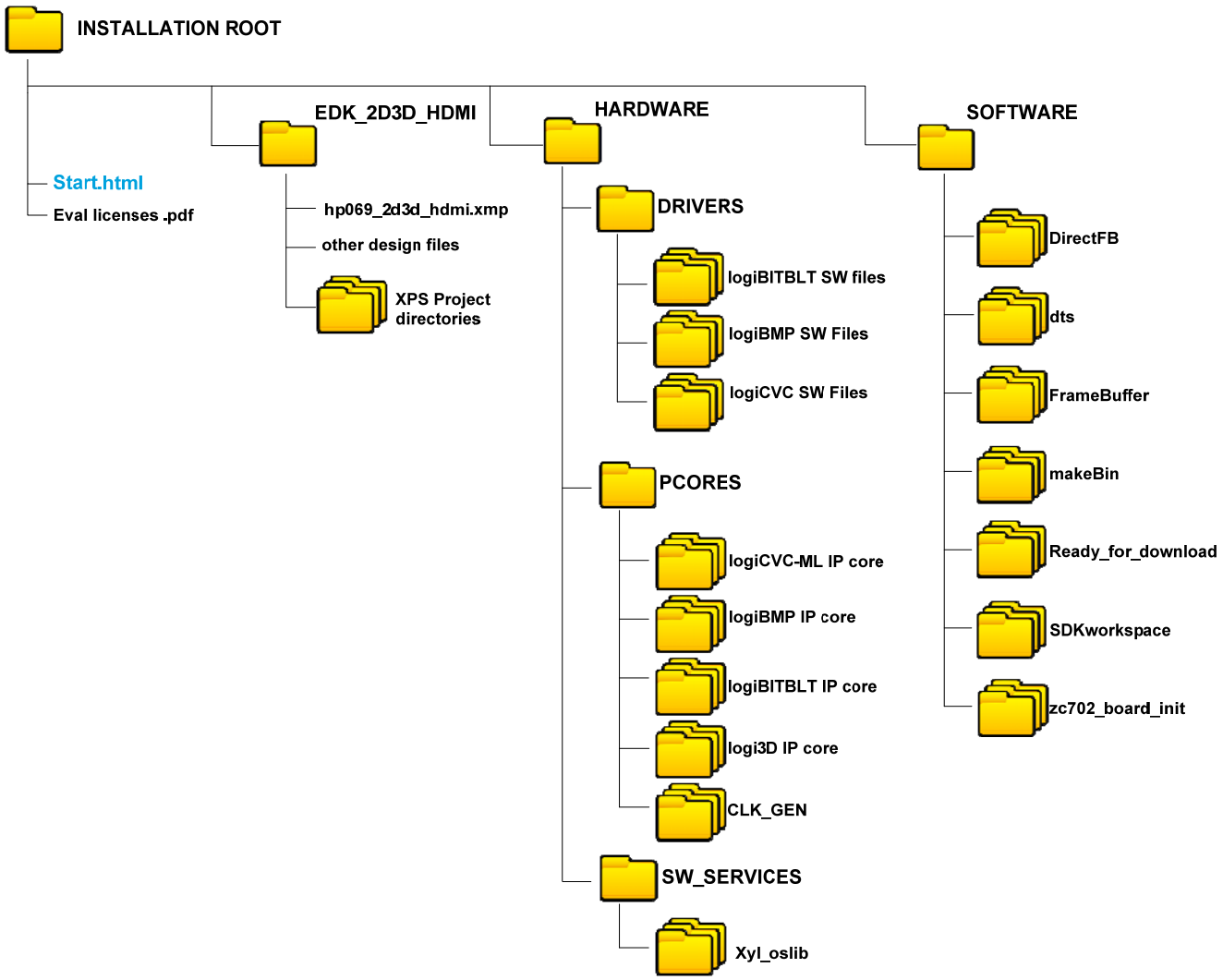


Figure 14: Directory Structure

Directory		Purpose
Installation Root		This directory contains the START.HTML page – the jump-start navigation page through the reference design.
EDK_2D3D_FMC		This directory contains the complete XPS project
	Design files	XPS files – use the hp069ad_2d3d_fmc.xmp file to open the XPS project
	Design directories	XPS project related directories.
Hardware		
	Drivers	Standalone (bare-metal) drivers for logicBRICKS IP cores with documentation and examples
	Pcores	Evaluation logicBRICKS IP cores. IP cores' User's Manuals are stored in doc subdirectories.
	SW_services	xyl_oslib Xylon OS abstraction library for Xilinx Xilkernel embedded kernel – use in standalone (non-OS) applications
Software		
	DirectFB	Xylon DirectFB driver for 2D acceleration
	dts	Linux device tree configuration file
	FrameBuffer	Patch containing the Xylon framebuffer driver and instructions
	makeBin	Utility script for creating boot.bin file
	Ready_for_download	Prepared binaries ready for download
	SDKworkspace	Xilinx SDK workspace folder for building bare-metal applications
	Zc702_board_init	Bare-metal application for the initialization of the board

Table 1: Explanation of Directories in logiREF-ZHMI-FMC Reference Design

4 GETTING LOGICBRICKS EVALUATION LICENSES

The following pages describe the procedure for getting and licensing evaluation logicBRICKS IP cores that takes several minutes to complete. If you experience any troubles during this process, please contact Xylon Technical Support Service – support@logicbricks.com.

You must be logged in to the Xylon website using your logicBRICKS user name and password to get an access to evaluation logicBRICKS IP cores. Unregistered users will be re-directed to the User Login page. Chapter 3.1 Registration Process explains this simple registration procedure.

Step 1 – Logged in users get the "My logicBRICKS" tab in the main www.logicbricks.com navigation menu. Click on it, and you will be directed to your main web page for communication with Xylon logicBRICKS – Figure 15. Please select the "**Request Eval IP Core**" tab in the left menu.

Figure 15: Step 1 – My logicBRICKS Navigation Page

Step 2 - Select the evaluation logicBRICKS IP core and click on "**Obtain evaluation license key**" link – Figure 16. If you are entitled to get the evaluation logicBRICKS IP core, you will be immediately asked (Figure 19) your Ethernet MAC ID number or Sun Host ID – as described in the Step 3.

If the evaluation logicBRICKS IP cores' list looks differently from the one shown on Figure 16, for example as the list presented by the Figure 17, please fill in and submit the request form (Figure 18), and allow us some time to process your request. Scroll down to get to the request form.

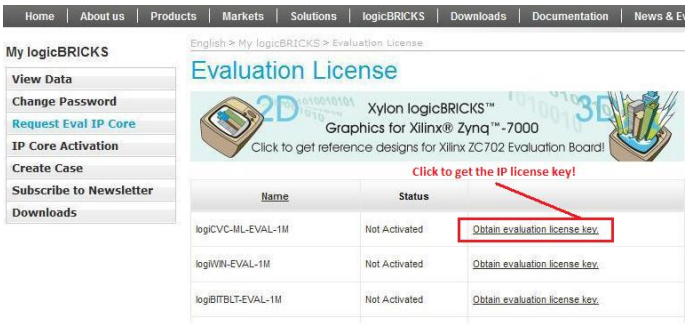


Figure 16: Step 2 – Selecting logicBRICKS IP Core for Licensing

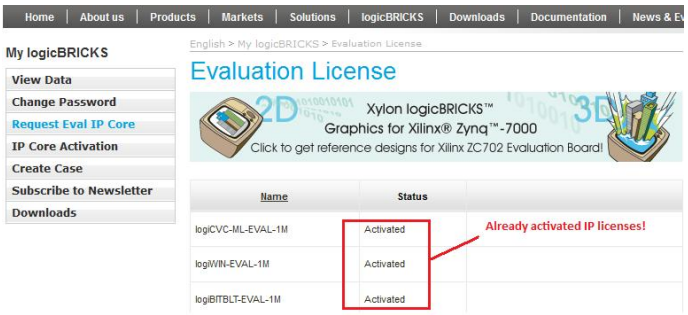


Figure 17: Step 2 – A List of Already Activated logicBRICKS IP Licenses

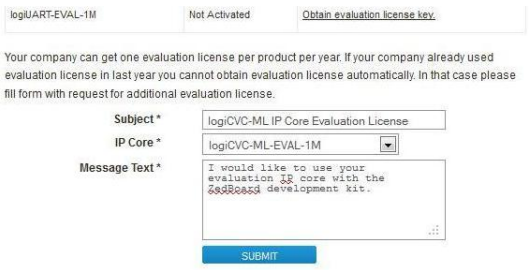


Figure 18: Step 1 - Licensing logicBRICKS Evaluation IP Cores

Step 3 - Evaluation logicBRICKS IP licenses are tied to your Ethernet MAC address or Sun Host ID (Figure 19), and can be used on a single working station only. Fill in this address and click on the "**Request License Key**" button. You should get the confirmation message – Figure 20. If you do not get the confirmation message, please contact Xylon technical support – support@logicbricks.com.

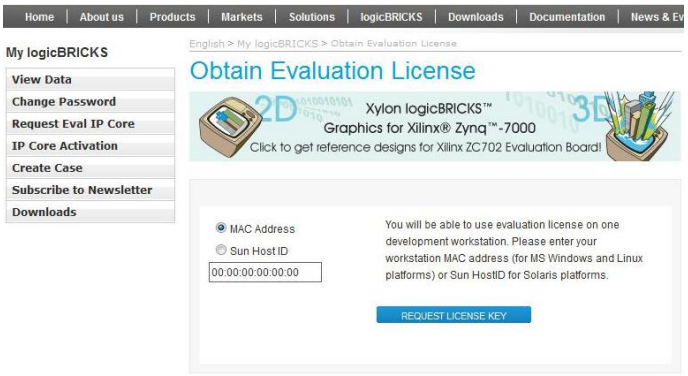


Figure 19: Step 3 - Licensing logicBRICKS Evaluation IP Cores

Figure 20: Step 3 – Confirmation Message

Step 4 - You will get an e-mail with the license key (file) and full instructions for setting up the license key and downloading the logicBRICKS IP core. Please follow the provided instructions.

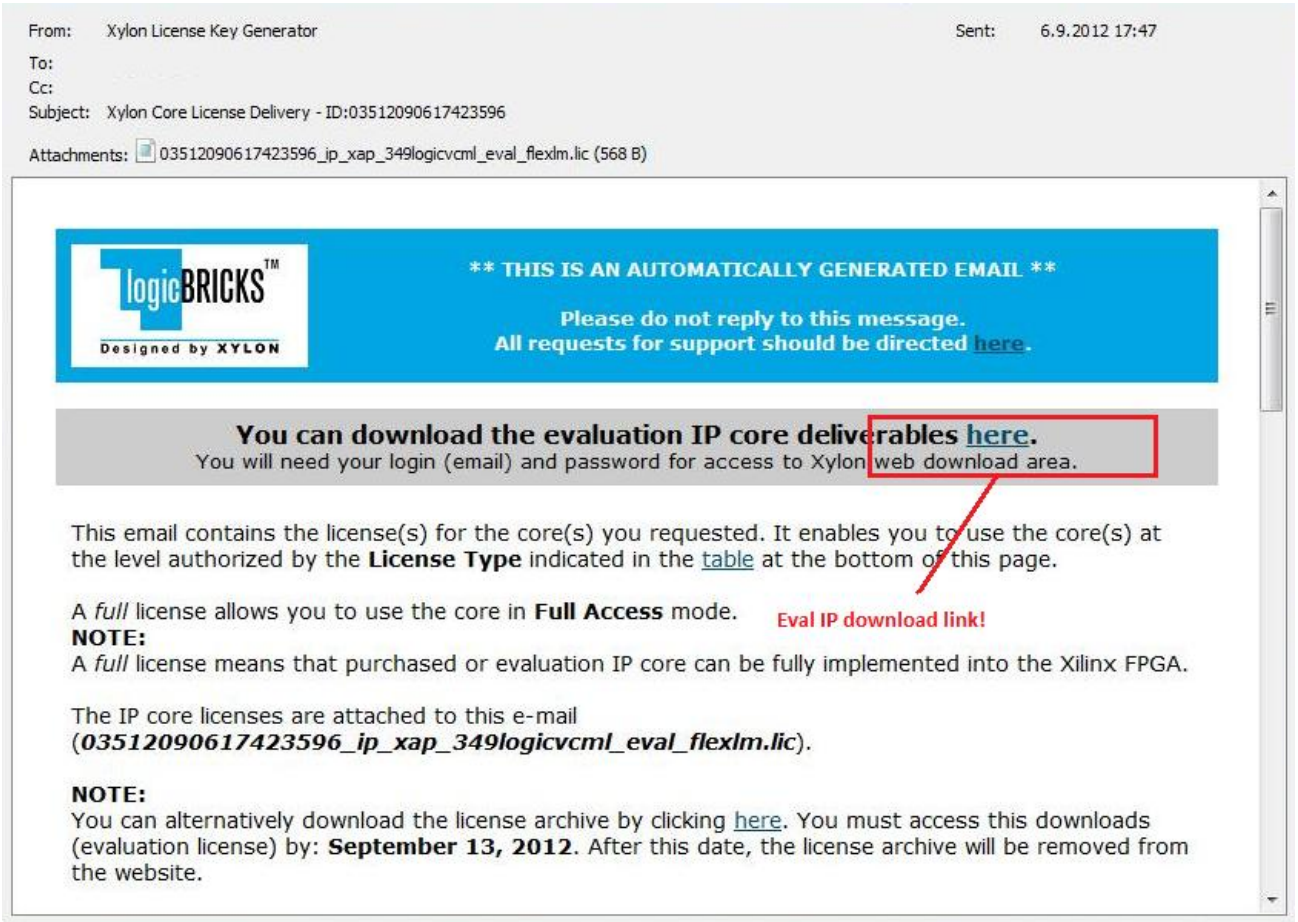


Figure 21: Step 4 – E-mail with logicBRICKS License and Download Instructions

5 LOGIREF-ZHMI-FMC DESIGN

The logiREF-ZHMI-FMC reference design for the Zynq-7000 EPP provides a work frame for development of HMI based embedded applications. logicBRICKS IP cores work as video frame grabber, graphics hardware accelerators, display and audio controller implemented in the Zynq-7000 programmable logic.

The reference design is based on the industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system controlling all system functions. Due to HMI graphics complexity, typical embedded MCUs (including the ARM) do not have enough computing performance to control the system and adequately render HMI graphics. The MCU typically require an aid from a dedicated hardware graphics controller that offloads the graphics rendering burden. Video processing requires implementation of the video frame grabber in programmable logic of the Zynq-7000 device.

Selected logicBRICKS IP cores for the reference design support different graphics functions. The Xilinx Platform Studio (XPS) and the EDK tools fully support the logicBRICKS IP cores and users can access them in a same manner as Xilinx IP cores from the EDK IP catalog.

The FPGA reference design implements fully featured 2D and 3D graphics controller integrating different graphics features, including bitmaps operations, alpha blending, overlays, rotations, scaling, LCD display control, 3D rendering, etc.

Any graphics controller has a display controller driving displays with various resolutions, timing requirements, and color depths. The logiCVC-ML Compact Video Controller carries out this function with the FPGA. This logicBRICKS™ IP core directly interfaces ADV7511 - High-Definition Multimedia Interface (HDMI®) transmitter.

Efficient graphics controllers implement different sorts of graphics accelerators. The logiBITBLT Bit Block Transfer IP core is a 2D graphics accelerator supporting complex bitmap operations like copying, moving, alpha blending, and Porter & Duff compositing operations between different graphics objects. For 3D graphic acceleration there is the logi3D IP Core - graphics accelerator IP core designed to support the OpenGL® ES 1.1 API. The logiBITBLT and the logi3D IP cores support smooth transitions and animations.

logiWIN Versatile Video Input IP core implements the frame grabbing feature. This IP core receives video stream from the camera placed on the FMC-HMI peripheral board. Video is further scaled, cropped and stored into video memory.

The logiREF-ZHMI-FMC reference design utilizes Xilinx AMS technology for four-wire resistive touch display control. Several audio inputs and outputs can be controlled through the logiI2S Audio Data Receiver/Transmitter IP core. Audio codecs, video camera, LCD display with touch screen are placed on the FMC-HMI peripheral board.

The memory subsystem is an essential part of any graphics based system. It must ensure the design has a fast memory bandwidth and enough storage space for GUI elements and application code. The logiREF-ZHMI-FMC (ZC702) includes 4x 8-bit DDR3 SDRAM memories connected as one 32-bit module, 1GB, interfaced by the Zynq.

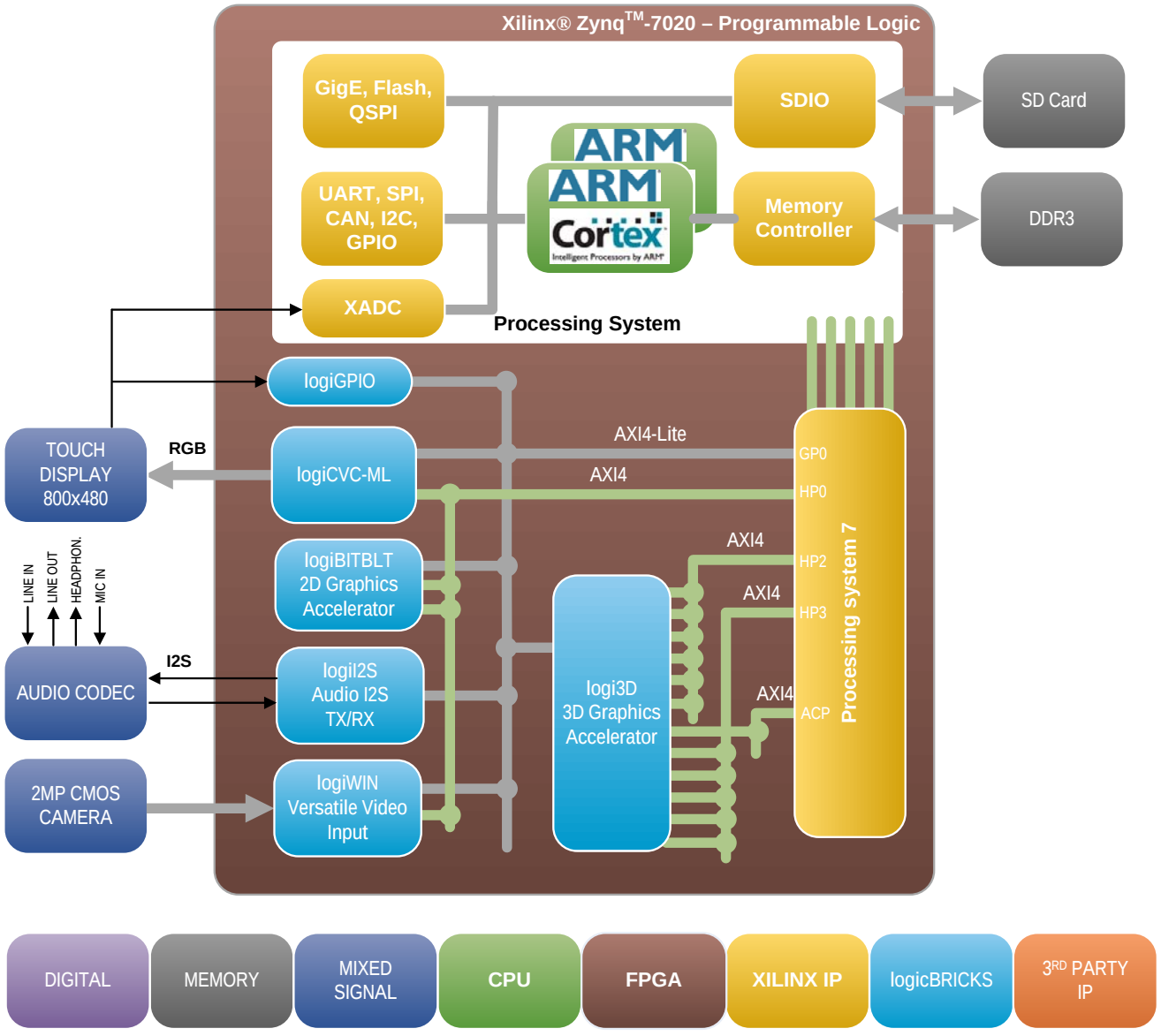


Figure 22: logiREF-ZHMI-FMC Reference FPGA Block Diagram

(Clock Generator Module and other utility IP cores are not shown)

5.1 Design Customization

The provided reference design can be customized in different ways. Please note that any changes in the provided reference design require evaluation IP licenses for logicBRICKS IP cores. The licensing process is described in the paragraph 4, Getting logicBRICKS Evaluation Licenses.

Possible design changes include:

- Change logicBRICKS IP settings, i.e. change number of graphics layers controlled by the logiCVC-ML display controller IP core
- Remove some logicBRICKS IP cores, i.e. remove all graphics accelerators and use only the logiCVC-ML display controller IP core, or remove the 3D acceleration and work with the 2D graphics only, etc.
- Add more instances of logicBRICKS IP cores, i.e. add second logiCVC-ML IP core and drive two displays with different graphics content
- Add your own or third-party IP cores to various combinations of logicBRICKS IP cores
- …

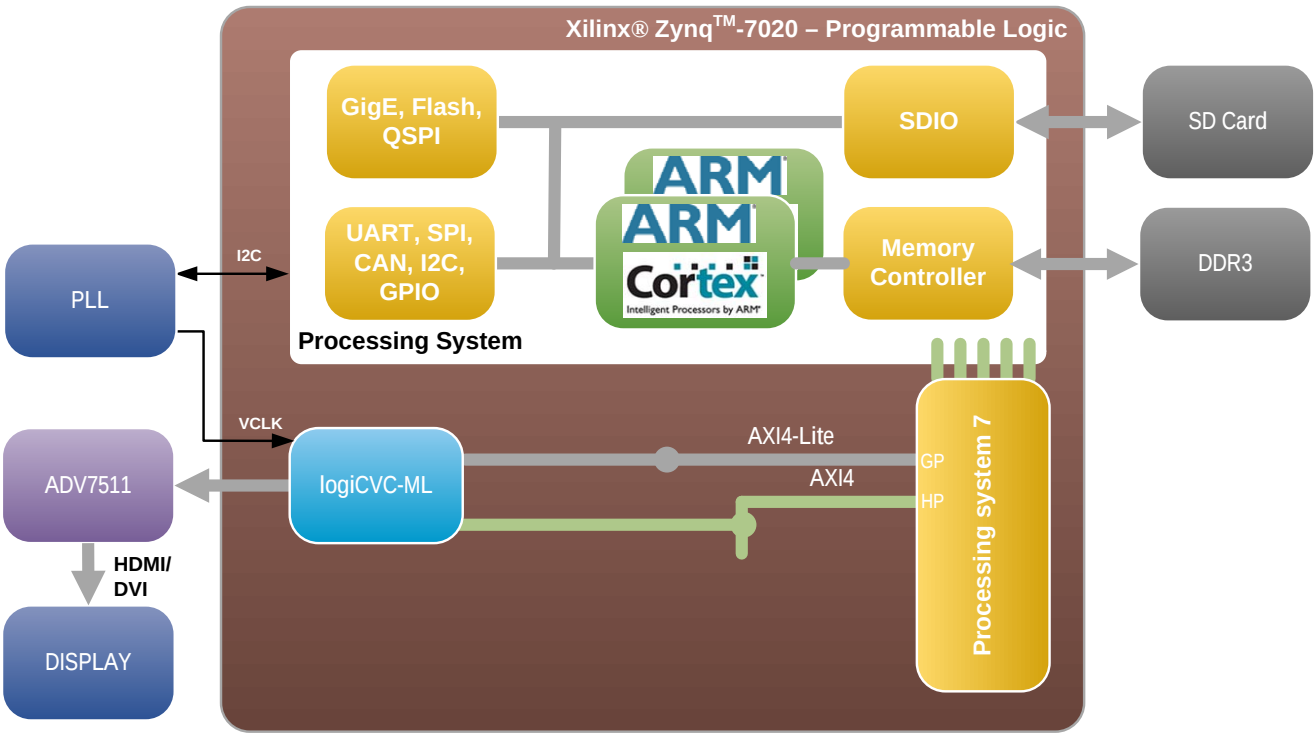


Figure 23: A Minimal Zynq-7000 AP SoC Display Controller

Figure 23 shows an example architecture featuring only the logiCVC-ML display controller IP core. Such a configuration provides no graphics acceleration in the programmable logic and all graphic contents must be fully drawn by the Processing System (PS). The consumption of programmable logic resources is minimal. The Figure 23 shows a clocking structure detail – please see the paragraph 6. Video Output Clocking.

5.2 logREF-ZHMI-FMC Memory Layout

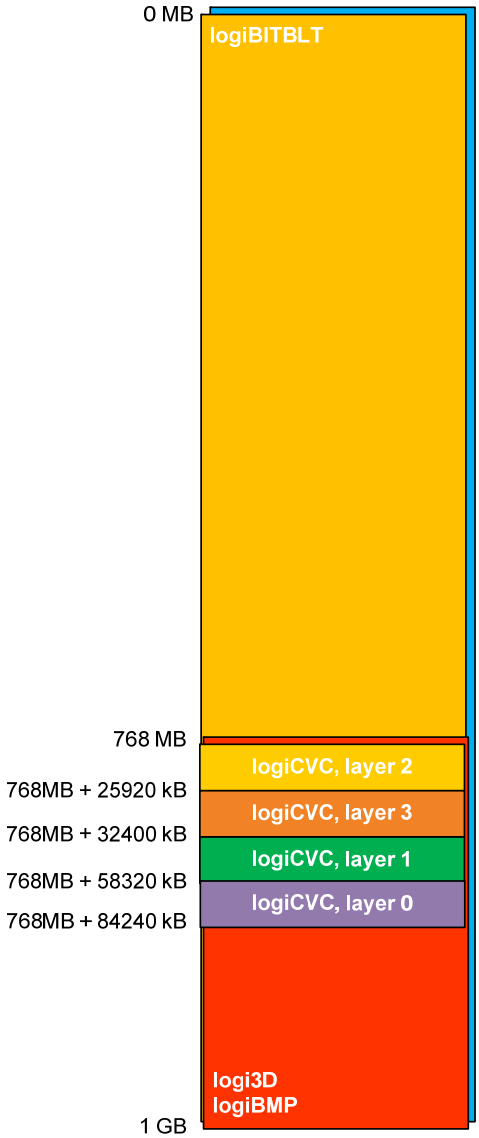


Figure 24: logiREF-ZHMI-FMC Memory Layout

Table 1: logicBRICKS IP cores' Memory Addressing

IP Core	Memory Access [MB]	Memory Stride [pixels]	Display Memory [HxV pixels]
logiCVC	768 – 1023	1024	up to 1024x1024
logiBITBLT	0 – 1023	1024	-
logiBMP	768 – 1023	1024	-
logi3D	768 – 1023	1024	-

6 VIDEO OUTPUT CLOCKING

Xylon's standard logiCVC-ML Compact Multilayer Video Controller IP core supports display resolutions up to 2048 x 2048. For information about support for higher display resolutions, please contact Xylon at info@logicbricks.com.

The logiREF-ZHMI-FMC reference design demonstrates the logiCVC-ML IP core implemented in Zynq-7000 AP SoC programmable logic. The logiCVC-ML display controller drives inputs into an Analog Devices ADV7511 HDMI Transmitter, which provides a digital video interface to the ZC702 Board. This 225MHz transmitter is HDMI 1.4- and DVI 1.0-compatible supporting 1080p60 with 16-bit, YCbCr, 4:2:2 mode color. ADV7511 HDMI Transmitter driver is integrated with the Xylon Framebuffer driver for the Linux OS. ADV7511 HDMI Transmitter driver is also provided for the bare-metal applications see the `zc702_board_init` application.

Xylon logicBRICKS IP cores and provided software can be used in many different hardware setups, and with many different display types. Therefore, in order to be able to fully utilize the graphics provided with the reference design for the ZC702 Board and to properly use logicBRICKS products in other hardware setups, designers should understand the video clocking scheme implemented in the logiREF-ZHMI-FMC reference design.

6.1 logiCVC-ML - Standard Display Resolutions and Pixel Clock

For full information about setting up the display interface controlled by the logiCVC-ML Compact Multilayer Video Controller IP core, please refer to the IP core's User's Manual. This chapter focuses on the pixel clock generation and control, since it depends on the overall system's architecture to a great extent.

Table 3 shows required pixel clock's frequencies for several popular display resolutions. Properly implemented display interface must respect the expected display signals' timings, which are based on the requested pixel clock. Wrong pixel clock causes wrong timings on the display interface and, as a consequence, wrong or missing picture on the display. It is visible from the table that graphic controller must be able to source different pixel clocks in order to support multiple display resolutions.

Resolution (@60Hz)	Pixel Clock (MHz)
VGA (640x480)	25.25
480p (720x480)	27
WVGA (854x480)	32
SVGA (800x600)	40
XGA (1024x768)	65
WXGA (1280x768)	68.25
HD 720p (1280x720)	74.25
HD 1080i (1920x1080)	74.25
SXGA (1280x1024)	108
HD1080p (1920x1080)	148.5

Table 3: Pixel Clock - Common Video Resolutions

The logiCVC-ML internal structure is shown on the block diagram on Figure 25. The VCLK clock signal controls all circuits inside the logiCVC-ML IP core, except the video memory subsystem (PLB, XMB or AXI4) related circuits and registers (OPB, PLB or AXI4). The VCLK clock signal frequency should be set according to the video display resolution.

The pixel clock output, PIX_CLK is proportional to the VCLK clock input and to control bits in the DTYPE and CTRL registers (please refer to the logiCVC-ML User's Manual, Chapter 10.2 Register Description).

A special clock module is requested outside of the logiCVC-ML IP core to support the functionality of adjustable PIX_CLK clock frequencies (changeable display resolutions). In this reference design external programmable PLL SI570 is in use. For more details please refer to si570.pdf.

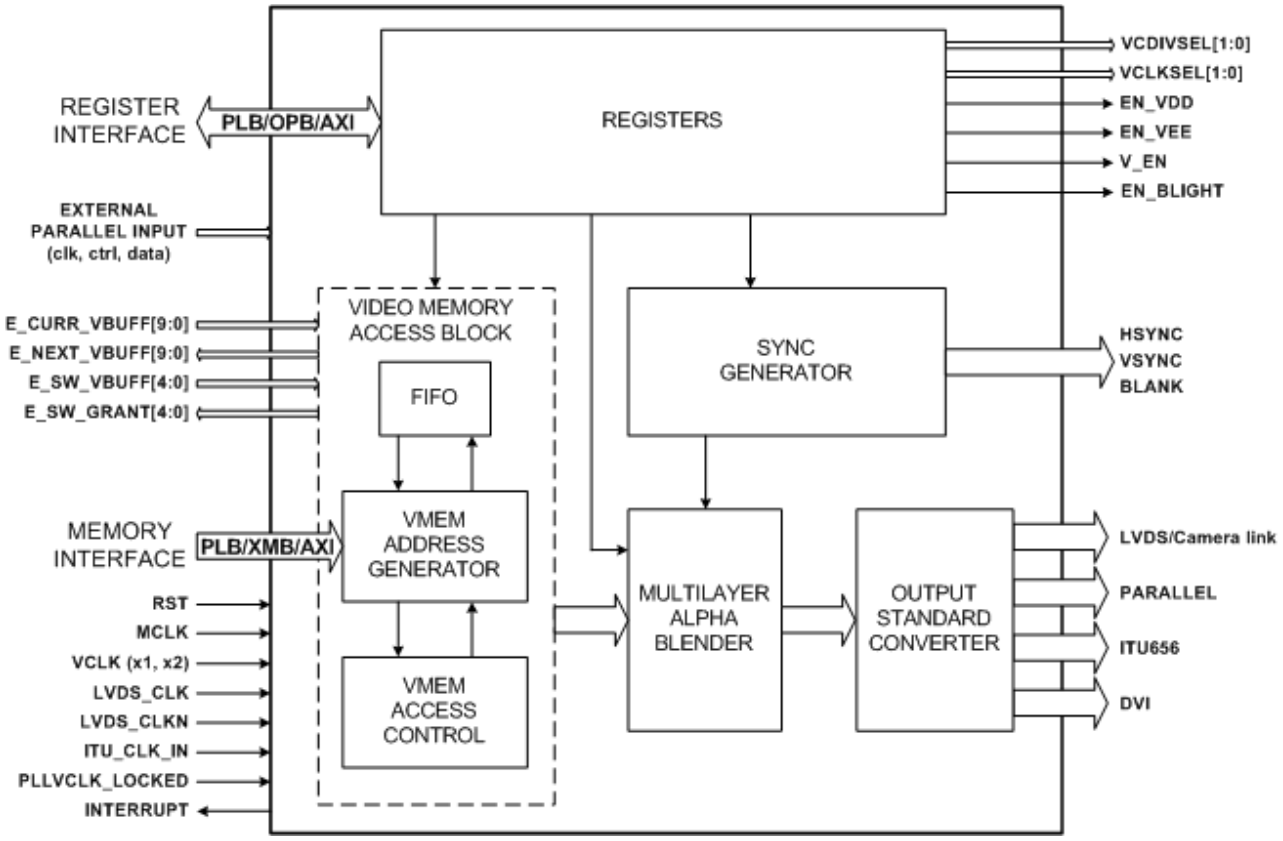


Figure 25: logiCVC-ML Architecture

6.2 Linux Frame Buffer – Changing Display Resolutions

Linux Framebuffer is a standard Linux driver that abstracts the graphics hardware and allows application software to access it through a well-defined interface. Software designers can use it with no need to know anything about the underlying hardware (IP cores) in Xilinx Zynq-7000 EPP or FPGA device.

The Linux Framebuffer delivered with the logiREF-ZHMI-FMC reference design is adopted by Xylon to fully support the logiCVC-ML display controller IP core.

Xylon framebuffer driver is located on Xilinx git server. Latest framebuffer driver version is provided in this installation, for instructions see `logiREF-ZHMI-FMC Installation Root/software/framebuffer/readme.txt`
Note that Xylon provides Device Tree Source `.dts` file with IP core configuration information specific to this referent design. When using the Linux kernel with this referent design user must use the Xylon dts/dtb files, located in the `logiREF-ZHMI-FMC Installation Root/software/dts` directory, instead of the ones provided by Xilinx. Figure 26 shows an excerpt from Xylon .dts file with commented explanations of the DTS structure.

```
xylon-video-params {
pixel-data-invert = <0>;
pixel-clock-active-high = <1>;
pixel-component-format = "ARGB";
pixel-component-layer = <0>,<1>,<2>;

/* index of logiCVC layer that will be used by the Linux console*/
active-layer = <3>;

/*Standard video mode (see /etc/fbmodes) can be selected here e.g. 640x480
   Also custom (dts) video mode can be selected here but it must be specified below.
  NOTE: When custom mode has the same name as standard mode then
  Custom mode prevails */
videomode = "1024x768"; /* default video mode selection – standard mode used */
/* videomode = "800x480_TM050RBH01"; */  /* default video mode selection – custom mode used

/* custom (dts) video mode definition – defined by the user if required */
800x480_TM050RBH01 {
name = "800x480_TM050RBH01";
refresh = <60>;
xres = <800>;
yres = <480>;
pixclock-khz = <30000>;
left-margin = <40>;
right-margin = <40>;
upper-margin = <29>;
lower-margin = <13>;
hsync-len = <48>;
vsync-len = <3>;
sync = <0>;
vmode = <0>;
};

/* NOTE: multiple custom(dts) video modes can be defined  here*/
};
```

Figure 26: Video Mode Definitions – An Excerpt from the Linux .dts

7 QUICK START

7.1 Required Hardware

A full evaluation of the provided reference design requires:

- ZC702 development kit*
- Xilinx FMC-HMI board
- HDMI or HDMI to DVI video cable (for 1024x768 capable monitor)
- SD card (min 256MB)
- A keyboard (USB Micro-B cable), or a control serial link (USB Uart or Ethernet) between PC and the ZC702 Board

- **optional**: USB Micro-B cable, USB hub, mouse and keyboard
- **optional**: MINI USB cable for debug UART
- **optional**: Ethernet cable for Telnet connection
- **optional**: Xilinx JTAG Parallel cable USB for standalone application development

* The reference design has been tested on the ZC702, Rev B

7.2 Xilinx Development Software

The logiREF-ZHMI-FMC reference design and Xylon logicBRICKS IP cores are fully compatible with Xilinx development tools – Xilinx Design Suite 14.2. Future design releases shall be synchronized with the newest Xilinx development tools.

Licensed users of Xilinx tools can use their existing software installation for the logiREF-ZHMI-FMC evaluation. Suitable ISE Design Suite versions are: Embedded and System Edition.

7.3 Set Up Linux System Software Development Tools

A set of ARM GNU tools are required to build the Linux software and applications. The complete tool chain for the Zynq-7000 All Programmable SoC can be obtained from the Xilinx ARM GNU Tools wiki page: http://wiki.xilinx.com/zynq-tools. Access to tools requires a valid, registered Xilinx user login name and password.

7.4 Set Up git Tools

Git is a free Source Code Management (SCM) tool for managing distributed version control and collaborative development of software. It provides the developer a local copy of the entire development project files and the very latest changes to the software.

Visit http://wiki.xilinx.com/using-git to get instructions how to use Xilinx git.

7.5 Set Up the ZC702 Board for Use with Precomiled Linux Demos from the SD Card

Xylon provides Linux, DirectFB and 3D demo binaries in the `software/ready-for-download/linux_sd` folder. If you want to run prepared demos, copy the content of the `SD_2D3D_FMC` directory to the root directory on the FAT32 formatted SD card.

For the most comfortable work with the precompiled Linux Demos, Xylon recommends use of a keyboard and a mouse connected through an USB hub to the ZC702 Board.

Set up your ZC702 Board as shown on the Figure 27:

- set the jumpers identically to the settings shown on the figure
- connect power supply, serial cable to the USB UART (optional), mouse and keyboard to the USB (OTG), Ethernet cable, HDMI cable
- plug in the SD card

Jumpers settings for the SD boot mode:

Board rev B.

Jumper	Setting
J21	2-3
J20	2-3
J22	1-2
J25	1-2
J26	2-3

Board rev D.

SW16	Setting
1	UP
2	DOWN
3	DOWN
4	UP
5	UP

Table 3: Jumpers Set Up for Booting from the SD Card

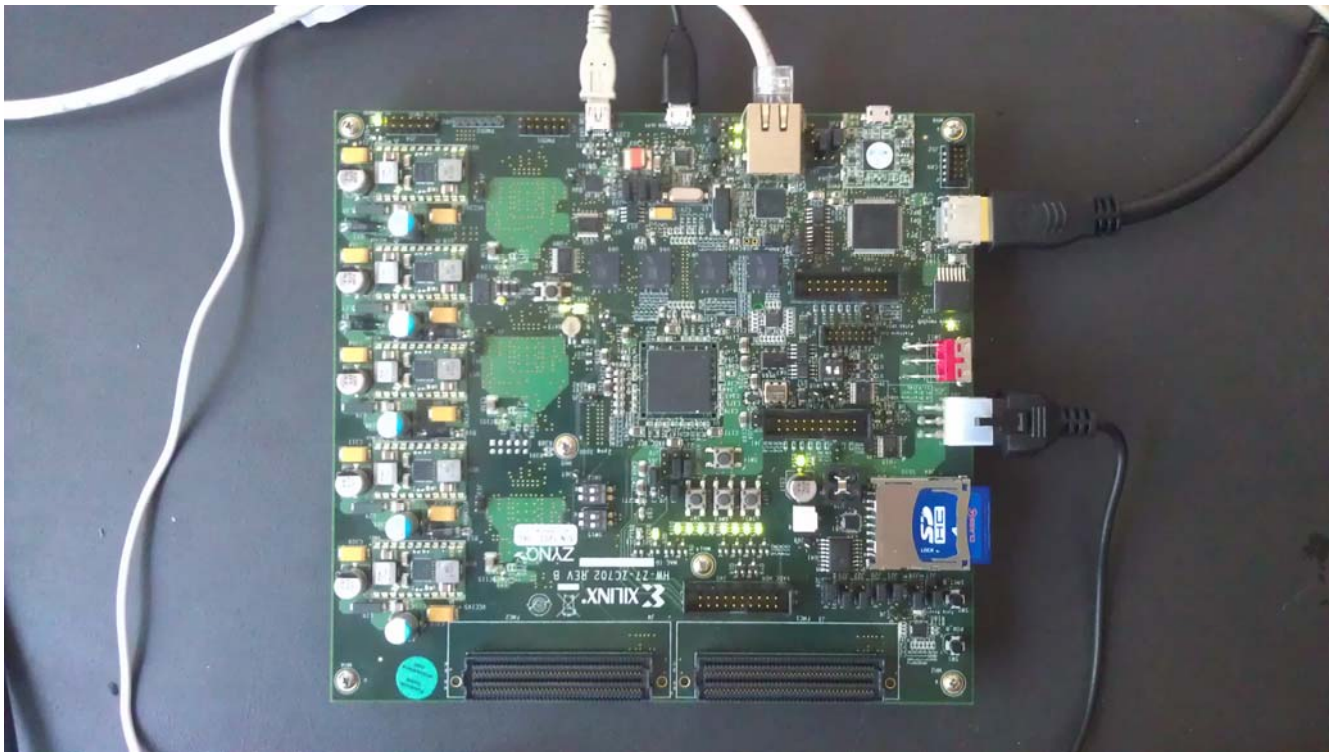


Figure 27: The ZC702 Board (Rev B) Setup for the logicBRICKS Reference Design

For full explanation of the ZC702's features and settings, please check the documentation Xilinx UG926.

7.6 Running Precompiled Demos from the SD Card Image

To quickly start precompiled Linux demos, make sure that you have the SD card with the precompiled image plugged in the board's slot, and all jumpers setup as described in the paragraph 7.5.

To control precompiled demos, you can:

- use the keyboard connected to the micro-USB port and write commands directly to the screen console
- use serial terminal program (baud rate 115,200) and USB UART connection to the ZC702 Board
- use telnet connection (IP address: 192.168.0.77) and Ethernet connection with the ZC702 Board

7.6.1 Running 3D Demo Apps

In the screen console, type in:

```
cd mnt
```

```
. run3d.sh
```

These commands start the demo. Control demos by keys A or D (left-right), E (select), and Q (quit). In some demos you can also use keys W, X, R and F. If you control the demo through the serial, or the Ethernet communication link, press ENTER after each key. CTRL+C key combination stops the demo.

7.6.2 Running 2D Demo Apps

In the screen console, type in:

```
cd mnt
. startdfb.sh
./df_texture  #control with the mouse, quit with 'Esc' not with CTRL-C
./df_knuckles #control with the mouse, quit with 'Esc' not with CTRL-C
./df_andi     #control with the keyboard, quit with 'Esc' not with CTRL-C
./df_dok         # quit with 'Esc' not with CTRL-C, observe CPU usage
results!
# run some other DirectFB demos ...
```

8 SOFTWARE DOCUMENTATION

Please use the `start.html` file (section 4. Software documentation), or open directly `/software/readme.html` file to find relevant documentation for using logiREF-ZHMI-FMC software deliverables. This file contains links to software documents and instructions related to:

- Standalone (Bare-Metal) software
- Linux software

8.1 Software Instructions – Standalone Software

- FSBL instructions
- Standalone software drivers (code and documentation) and examples
- Zc702_board_init application, HDMI initialization and pixel clock setting
- Building standalone applications
- Running standalone applications with the ZC702 Board setup for standalone applications

8.2 Software Instructions – Linux Software

Xylon provides Linux frame buffer driver, DirectFB driver and OpenGL ES 1.1 library/driver for Linux. Zynq toolchain, Linux kernel and file system used for development and demonstrations of Xylon drivers are provisions of Xylon.

- Xylon frame buffer driver; Linux kernel building instructions, and DTS files
- Xylon DirectFB driver; general information and building instructions
- Xylon 3D graphics acceleration library; binaries, instructions for building 3D applications, code examples
- Running Linux applications with the ZC702 Board setup for the precompiled SD card image

9 REVISION HISTORY

Version	Date	Author	Approved by	Note
1.00.a	July 5, 2012	Z. Šafaržik		Initial
1.01.a	October 5, 2012	Z. Šafaržik, G. Galić, G. Pantar		Updated chapter: "Introduction" Added chapters: "Get and Install the Reference Design" "Getting logicBRICKS Evaluation Licenses" "Video Output Clocking" "Quick Start" "Software Documentation"