Xylon d.o.o.

Fallerovo setaliste 22
10000 Zagreb, Croatia
Phone: +385 1 368 00 26
Fax: +385 1 365 51 67
E-mail: support@logicbricks.com
URL: www.logicbricks.com

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Please contact Xylon
Reference Designs & Application Notes	Please contact Xylon
Additional Items	FatFs – Generic FAT File System Module OS-independent IP SW driver
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 AP SoC, 7 Series and older Xilinx FPGA families
- Plug-and-Play Standard and High Capacity SD cards to Xilinx All Programmable devices
- Secure Digital Host Controller compliant with Secure Digital Specifications Version 2.00
- Evaluation IP core available online
- Programmable transfer rates up to the maximum data rate specified by the standard (25 MB/sec and 50 MHz bus frequency)
- Supports non-DMA, standard DMA and Xylon's custom DMA data transfers
- The standard DMA supports enhanced features:
  - Read/write memory burst cycles (16, 32 or 64 clock cycles)
  - Interrupted memory burst cycles
  - Byte address boundary memory accesses
  - DMA interrupt mechanism compliant to the supported SD standard

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LCs	Slices[1] (FFs/LUTs)	IOB[2]	BRAM	MULT/ DSP48/E	Design Tools
	mclk	sd_base_clk[3]	rclk						
Artix®-7 (XC7A35T-1)	130	100	160	4070	636 (1143/1578)	6	2	0	Vivado 2014.4
Kintex®-7 (XC7K70T-2)	150	100	180	3846	601 (1143/1579)	6	2	0	Vivado 2014.4
Virtex®-7 (XC7V585T-3)	180	100	200	3808	595 (1143/1580)	6	2	0	Vivado 2014.4

Notes:
1) Assuming the following configuration: AXI4-Lite registers interface, 32-bit AXI4 memory interface for standard DMA and 32 clock cycles burst.
2) Assuming only SD Card interface signals are routed off-chip, auxiliary signals, register and memory interface are connected internally.
3) Maximum sd_base_clk frequency according to Secure Digital Specification Version 2.00 is 100 MHz.

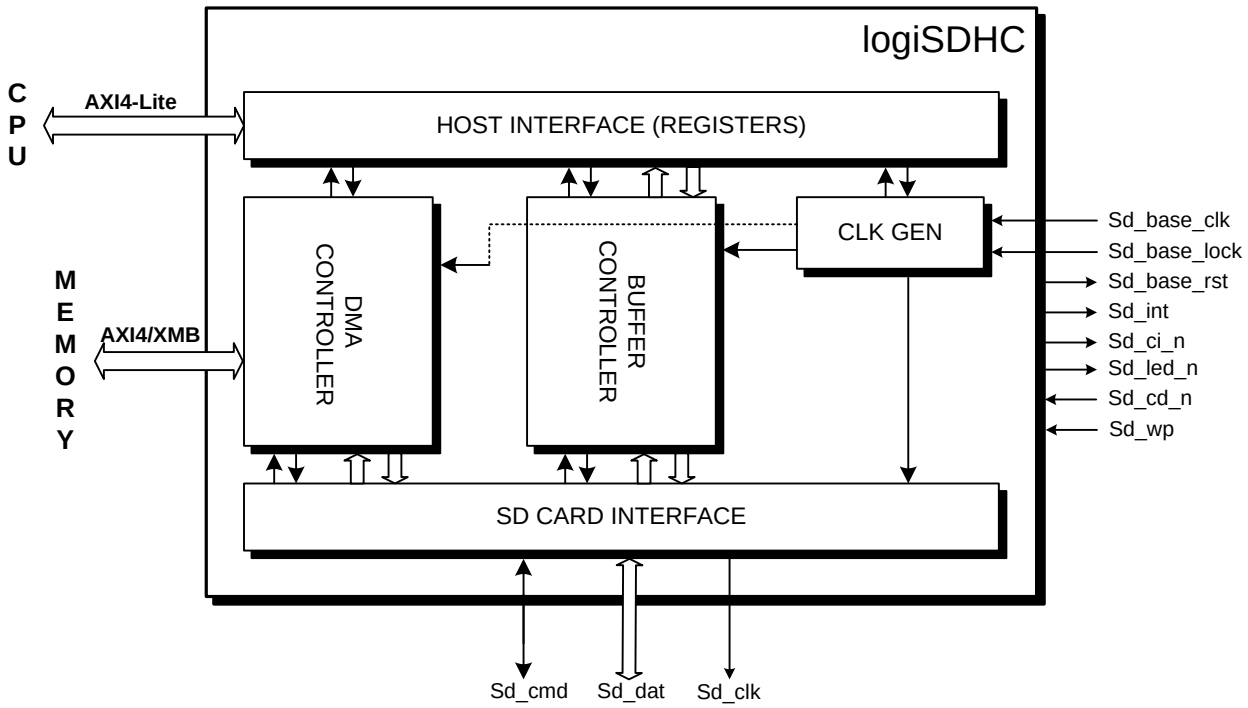

Figure 1 : logiSDHC block schematic

Features (cont)

- Xylon's custom DMA supports:
  - Accelerated read (SD Card to Host) transfers of bitmap files
  - Read memory burst cycles (16, 32 or 64 clock cycles)
  - Interrupted memory burst cycles
  - Byte address boundary memory accesses
  - DMA interrupt generated at ends of completed transfers
- Both DMA engines support Little and Big Endian host systems
- ARM® AMBA® AXI4-Lite register interface (32 bits)
- DMA memory interface (32 bits) designed for ARM AMBA AXI4 interface
- Buffer overflow detection of too fast read transfers which cannot be handled by the host
- Read wait stalls too fast read transfers and prevents buffer overflows on the host's side
- Parametrizable VHDL design that allows tuning of slice consumption and features set through the GUI
- Xilinx Vivado® IP Integrator compatible IP version supports the 7 Series and Zynq-7000 AP SoC
- Xilinx ISE® Platform Studio compatible IP version supports older Xilinx FPGA families
- Simple Plug'n'Play with other Xylon logicBRICKS, Xilinx and third-party IP cores
- Deliverables include Generic FAT File System Module – FatFs (http://elm-chan.org/fsw/ff/00index_e.html)

Applications

Electronic devices serving different vertical markets and requiring big and fast non-volatile storage:

- Consumer
- Automotive
- Industrial
- Medical
- Military, etc.

General Description

The logiSDHC is the Secure Digital (SD) card Host Controller IP core from the Xylon's logicBRICKS IP core library optimized for Xilinx All Programmable devices. It is designed to transfer data from the system memory to the SD card's data bus, and vice versa. The IP core enables expansion of embedded systems based on the Xilinx FPGA devices by mass storage capabilities.

The logiSDHC IP core is SD Host Controller Standard Specification Version 2.00 compliant. The IP is a memory IO mapped hardware module providing a general-purpose interface between the embedded SW application and the SD card memory component.

The logiSDHC IP core supports non-DMA and DMA data transfers. Implemented DMA mechanisms enable fast data transfers and require minimal CPU activities. Two DMA mechanisms are supported: the standard DMA mechanism compliant to the SD Host Controller Standard Specification and the custom Xylon's DMA mechanism optimized for bitmaps reading from the SD card.

Xylon's DMA transfers RGB formatted bitmaps and AVI (uncompressed) files and converts them into ARGB data formatted for Xylon's graphics and video IP cores, such as the logiCVC-ML Compact Multilayer Video Controller (http://www.logicbricks.com/Products/logiCVC-ML.aspx).

The DMA is an optional feature and can be switched off to preserve available FPGA resources.

To purchase the IP, or to download the evaluation logiSDHC IP core, please visit:

http://www.logicbricks.com/Products/logiSDHC.aspx.

Functional Description

The Figure 1 presents internal logiSDHC architecture. The logiSDHC functional blocks are: Host Interface, Clock Gen, Buffer Controller, DMA Controller, SD Card Interface.

Host Interface

Implements register interface according to the SD Specification Version 2.00. The host interface controls the functionality of the logiSDHC IP core through a set of control and command signals.

Clock Gen

Generates clock and clock enable signals for IP's sub modules and for the SD Card.

Buffer Controller

Manages non-DMA data transfers.

DMA Controller

The DMA enables fast transfers to/from the system memory and the SD card. Bursts of data are buffered in Read and Write buffers that regulate data formatting and transfers between different clock domains.

SD Card Interface

The card interface implements separated state machines. One state machine responses to system commands and handles SD card's responses, while the other one handles data transfers to/from the memory card.

Core Modifications

The core is supplied in an encrypted VHDL format which allows the user to take full control over configuration parameters. Various logiSDHC configuration parameters are selectable prior to VHDL synthesis and can be setup through Xilinx implementation tools GUI. The following table (Table 2) presents some configuration parameters selected from a list of the available parameters:

Table 2: logiSDHC VHDL configuration parameters

Parameter	Description
C_USE_DMA	0 – DMA controller not implemented 1 – DMA controller implemented
C_DMA_TYPE	0 – SD card 2.0 spec. DMA controller 1 – Xylon type DMA controller
C_MEM_INTERFACE	Only AXI4 memory interface supported for Vivado
C_REGS_INTERFACE	Only AXI4-Lite interface supported for Vivado

For the complete list of parameters, please consult the logiSDHC User's Manual delivered with the IP core.

The logiSDHC is designed with regard to SD Specification Version 2.00. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiSDHC core or to supplement some of your specific functions, you can allow us to tailor the logiSDHC to your requirements. The logiSDHC source code (VHDL sources) is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Memory Interface		
AXI4 Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Register Interface		
AXI4-Lite Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
SD Card ports		
SD_CLK	Output	SD Card clock
SD_DAT	Input/Output	SD Card data
SD_CMD	Input/Output	SD Card command
Auxiliary signals		
SD_BASE_RST	Output	SD base clock DCM reset
SD_BASE_LOCK	Input	SD base clock DCM lock
SD_BASE_CLK	Input	SD base clock
SD_INT	Output	SD interrupt
SD_WP	Input	SD write protect switch
SD_CD_N	Input	SD card not present
SD_CI_N	Output	SD card not inserted
SD_LED_N	Output	LED indicating that SD Card is in use

Verification Methods

The logiSDHC is fully supported by the Xilinx Vivado IP Integrator and Xilinx Platform Studio integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiSDHC implementation does not require any particular skills beyond general Xilinx tools knowledge. If you wish to simulate this IP, please contact Xylon.

The logiSDHC evaluation IP core can be downloaded from Xylon web site and be fully evaluated in hardware.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon provides several free pre-verified video and graphics reference designs for the most popular Xilinx Zynq-7000 AP SoC based evaluation kits: Xilinx ZC702 and ZC706, MicroZed™ and ZedBoard™ from Avnet Electronics Marketing. Design deliverables include: evaluation logicBRICKS IP cores, hardware design files prepared for Xilinx Vivado or ISE (XPS) design suite, complete Linux OS image, Xylon logicBRICKS software drivers for Linux OS and DirectFB, and demo software applications.

To learn more about the Xylon reference designs, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

To learn more about the Xylon reference designs and other ways of IP evaluation, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

Revision History

Version	Date	Note
1.00.a	06. 03. 2009.	Initial Xylon release – new doc template.
1.01.	29. 11. 2010.	Updated according to modifications made in the core version 1.01.a.
1.05.a	08. 06. 2011.	Added AXI support.
1.05.c	30. 09. 2011.	Timings statistics update.
1.06.a	27. 10. 2011.	Updated according to modifications made in the core version 1.06.a.
1.06.b	15. 12. 2011.	Updated according to modifications made in the core version 1.06.b.
1.07.	30. 01. 2013.	Added support for Artix-7 and Zynq 7000 AP SoC.
1.7.	09. 12. 2014.	Document updated with information about the Xilinx Vivado compatible logiSDHC IP core. Updated Table 2 and Table 3. Small corrections made throughout the document. New versioning scheme introduced for Vivado packaged IP core.