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Core Facts

Provided with Core	
Documentation	Datasheet
Design File Formats	Encrypted VHDL
Constraints Files	Reference design constraint files
Verification/Validation	Simulated and HW validated
Reference Designs & Application Notes	logiREF-VIDEO-HDR-ISP reference design for the Xylon logiUVK kit
Additional Items	logiUVK HDR UltraHD Video Kit
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim® Aldec Active-HDL™ and Riviera-PRO™	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC and 7 Series FPGAs
- Enables easy interfacing of Ultra HD CMOS image sensors to Xilinx All Programmable devices
- Supports Sub-LVDS interface and recognizes major Sony® IMX image sensor sync codes
- Fully compatible with the Sony IMX274 and IMX290 CMOS image sensors
- Can be adapted to other sensors with the Sub-LVDS interface and for the latest Xilinx devices
- Supported number of bus channels (differential pairs): 4, 6, 8, and 10
- Maximum input video resolution and frame rate are limited by the targeted FPGA family
- Validated with the Ultra High-Definition 4K2Kp60 (3840x2160@60fps) video inputs
- Supports Raw Bayer 10-bit and 12-bit video input and 8-bit,10-bit or 12-bit video output
- Enables parallel processing of 1, 2 or 4 pixels per clock
- Generates HSYNC, VSYNC and Reset signals for image sensors
- Video output is ARM® AMBA® AXI4-Stream protocol compliant
- Integrated an optional output image cropping
- Supports marking of two different exposures in the High-Dynamic Range (HDR) video input
- Configuration registers are AMBA AXI4-Lite protocol compliant
- Can be evaluated on Xylon logiUVK kit as a part of the 4K2K HDR UltraHD video pipeline reference design
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- Xylon assures maintenance and technical support

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LUT	FF	IOB	RAMB36	RAMB18	DSP48	PLL/ MMCM	BUFG/ BUFR	Design Tools
	aclk	s_axi_clk									
Zynq®-7000 (XC7Z045-2)	191	146	2338	3380	11	0	10	0	0	1	Vivado 2017.1

1) Assuming typical configuration: 10ch input, 288 MHz Sub-LVDS clock (DDR), 10bpc, Bayer input and output, 4 pix/clk, AXI4-Lite interface
2) Implementation statistics given for the Artix-7 and the Kintex-7 FPGAs are valid for the Zynq-7000 All Programmable SoC family
3) Implementation statistics can vary depending on implementation tool options, related FPGA design logic, device speed grade...

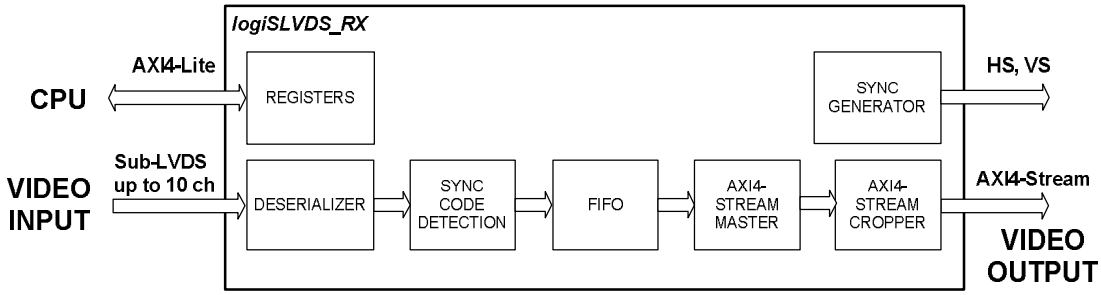

Figure 1: logiSLVDS_RX Architecture

Applications

Application fields include Surveillance, Automotive Driver Assistance, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

General Description

The logiSLVDS_RX IP core from the Xylon logicBRICKS IP library enables easy interfacing of ultra high resolution Sony CMOS image sensors to image signal processing pipelines and application processors implemented in Xilinx All Programmable devices. Xylon supports IP modifications and adaption for other image sensors through design services.

High speed data transfers are supported by the Sub-LVDS differential interface, which is a reduced voltage form of the LVDS signaling. The IP core can be configured to support up to ten (10) interface channels (differential pairs). It performs data deserialization, recognizes camera sync codes, optionally generates HSYNC and VSYNC signals required by the sensor, buffers pixels to decouple image sensor and the internal SoC bus, and outputs the video data packaged in compliance to the AXI4-Stream interface. The logiSLVDS_RX can also mark two different exposure video lines when used with the HDR image sensors. In order to support the highest possible input video resolutions, the logiSLVDS_RX IP core can be configured for parallel processing of 2 or 4 pixels per clock.

Figure 2: logiUVK Kit in the Transportation Case (not included with the kit)

The logiSLVDS_RX IP core is AMBA AXI4 bus protocol compliant and can be smoothly integrated with other Xylon logicBRICKS, Xilinx or third-party IP cores. The logiSLVDS_RX video output interface conforms to the

AXI4-Stream video protocol and assures low-latency video processing with no need for the external video frame buffering. An AXI4-Lite compliant registers interface assures high flexibility and enables processor to control the logiSLVDS_RX through registers.

The logiSLVDS_RX IP core is well suited for use with the logiISP Image Signal Processing (ISP) Pipeline and the logiHDR High Dynamic Range (HDR) Pipeline IP cores. Xylon advanced ISP pipelines support many image processing capabilities, such as removal of defective pixels, de-mosaicking of Bayer encoded video, image color and gamma corrections, advanced noise filtering, video analytics used for control algorithms like Auto White Balance and Auto Exposure, video data formats and color domains conversions, merging of different exposures for HDR enabled sensors and other HDR video enhancements.

All Xylon logicBRICKS IP cores are prepackaged for Xilinx Vivado IP Integrator (IPI) tool. They require no skills beyond general tools knowledge and can be used in the same way as Xilinx IP cores. Video system designers can easily setup the logicBRICKS IP cores, including the logiSLVDS_RX IP core, by setting up all IP core's parameters through an easy-to-use IPI GUI interface.

The logiSLVDS_RX and other Xylon image signal processing IP cores can be fully evaluated on the logiUVK HDR UltraHD Video Kit (Figure 2). To learn more about this development kit, please visit:

http://www.logicbricks.com/Products/logiUVK.aspx

Functional Description

The Figure 1 presents internal logiSLVDS_RX architecture. The logiSLVDS_RX performs deserialization of the input LVDS lines. The deserialized data are buffered in FIFOs in order to compensate for differences in the data rates of the input and the output stages of the IP core. The buffered video data is read by the AXI4-Stream block that packets the output video data. Optionally, the output video stream can be cropped.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator. Many logiSLVDS_RX configuration parameters are selectable prior to VHDL code synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiSLVDS_RX VHDL Configuration Parameters

Parameter	Description
C_NUM_CH	Number of Sub-LVDS channels: 4, 6, 8, 10
C_CH_WIDTH	Sub-LVDS channel data width (bits): 10, 12
C_HS_PERIOD	Default period of HSYNC signal, in number of ref_clk_in clock periods
C_HS_WIDTH	HSYNC pulse width
C_VS_PERIOD	Default period of VSYNC signal, in number of HSYNC signal periods
C_VS_WIDTH	VSYNC pulse width
C_COUNTER_WIDTH	HSYNC and VSYNC counters width
C_USE_HDR	Enable detection of different exposures in the input video data
C_MAX_SAMPLES_PER_CLOCK	Pixels per clock: 1, 2, 4
C_AXIS_DATA_WIDTH	Output pixel width: 8, 10, 12
C_RST_SELECT_ON_LAST	Use restart pixel position on every line
C_SAV_LEF	Define the code for start of active video in long exposure frame (HDR)
C_SAV_SEF	Define the code for start of active video in short exposure frame (HDR)
C_EAV_LEF	Define the code for end of active video in long exposure frame (HDR)
C_EAV_SEF	Define the code for end of active video in short exposure frame (HDR)
C_SAV_BLANK	Define the code for start of blanking line (HDR)

Parameter	Description
C_EAV_BLANK	Define the code for end of blanking line (HDR)
C_SAV_EAV_FSET_MASK	Define the code of mask indicating combined LEF and SEF frames (HDR)
C_USE_OUT_CROPPING	Enable/disable cropping module
C_X_CROP	Horizontal starting position for cropping
C_Y_CROP	Vertical starting position for cropping
C_X_WIDTH	Number of pixels in line, transferred after starting position pixel
C_Y_HEIGHT	Number of lines transferred after starting position line

The logiSLVDS_RX is designed with regard to adaptability to various sensors. However, there may be instances where source code modification is necessary. Therefore, if you wish to adopt the logiSLVDS_RX core to your specific needs and/or to supplement the IP core's features set, you can allow us to tailor the logiSLVDS_RX to your requirements.

Core I/O Signals

The core I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Streaming Video Interface		
AXI4-Stream Video Master Interface	Bus	Refer to Xilinx AXI Reference Guide
Control Interface		
AXI4-Lite Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
Clock and Reset Signals		
ref_clk_in	Input	Sensor clock, input to the receiver
io_clk_in_p	Input	Differential clock input (p) from the sensor
io_clk_in_n	Input	Differential clock input (n) from the sensor
io_clk_out	Output	Clock output from the deserializer
aclk	Input	AXI4-Stream clock, shared between all streaming interfaces
aresetn	Input	AXI4-Stream reset, active low, shared between all streaming interfaces
s_axi_aclk	Input	AXI4-Lite clock
s_axi_aresetn	Input	AXI4-Lite reset, active low
Sub-LVDS Interface		
io_data_in_p	Input	Differential data input (p) from sensor
io_data_in_n	Input	Differential data input (n) from sensor
Sensor Control Interface		
io_xvs	Output	Sensor VSYNC signal
io_xhs	Output	Sensor HSYNC signal
io_xclr	Output	Sensor reset signal

Verification Methods

The logiSLVDS_RX is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiSLVDS_RX implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Camera systems

Available Support Products

Xylon provides the logiREF-VIDEO-HDR-ISP free pre-verified reference design to showcase the logiSLVDS_RX IP core and Xylon ISP pipelines on the Xilinx Zynq-7000 AP SoC based logiUVK HDR UltraHD Video Kit. The reference design contains everything you need to immediately start evaluating and working with the Xylon logiSLVDS_RX: the SoC design including evaluation logicBRICKS IP cores, hardware design files, documentation and the GUI-based demo application (Linux OS):

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/HDR-ISP-Pipeline-for-Xilinx-All-Programmable.aspx

Xylon's logiISP-UHD Image Signal Processing Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx All Programmable devices. The logiISP-UHD ISP pipeline IP core can be supplemented with the logiHDR High Dynamic Range (HDR) Pipeline. To learn more about these IP cores, please visit:

URL: http://www.logicbricks.com/Products/logiISP.aspx
URL: http://www.logicbricks.com/Products/logiHDR.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiSLVDS_RX.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	February 19th, 2016	Initial release
1.1	August 23rd, 2017	Added 12-bit data width support. Added several generics for HDR video marking and an optional cropping module. Supports the latest Xilinx implementation tools.