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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	
Verification	
Reference Designs & Application Notes	Application note app0038
Additional Items	SW driver
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 AP SoC and FPGAs
- Drives up to 16 stepper motors using 8-bit PWM micro-step drive
- Supports MMT and Switec stepper motors
- Micro-stepping can achieve extremely precise resolution due to a programmable FPGA nature and IP's parameterized architecture
- Supports stepping for programmed number of steps and indefinite circling
- Supports different driving methods:
  - Full-Step Mode (Two-Phase-On)
  - Full-Step Mode (One-Phase-On)
  - Half-Step Mode
  - Micro-step Mode
- Supports DSP driving (HW Acceleration/Deceleration/Smoothing control) and direct control bypassing the DSP logic (Bypass mode)
- Programmable internal RAM tables for 8 different PWM characteristics optimized for specific motors
- An optional serialized output bus reduces a number of used FPGA pins
- Supports Return-To-Zero and Zero Position Detection
- Configurable CoreConnectTM OPB, PLB or AXI4-Lite bus interface
- Prepared for Xilinx Vivado® (IPI) and ISE® (XPS) Design Suits
- Parameterizable VHDL design that allows tuning of slice consumption and features set

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)	LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT	BRAM	MULT/ DSP48A1/E1	DCM / CMT	GTx	Design Tools
Spartan®-6 (XC6SLX45T-3)	100	3565	557 (984/1091)	42	0	2	4	0	N/A	ISE® 14.7
Artix 7 (XC7A100T-3)	200	2983	466 (982/1052)	42	0	2	4	0	N/A	ISE® 14.7
Kintex 7 (XC5VLX75T-2)	200	2836	443 (868/1080)	42	0	2	4	0	N/A	Vivado® 2014.2

Notes:
1) Assuming the following configuration: 4 motors support, 8192 microstep sweep, included Bypass logic, included output serializer and 32-bit AXI4-Lite register interface
2) Assuming register interfaces connected internally

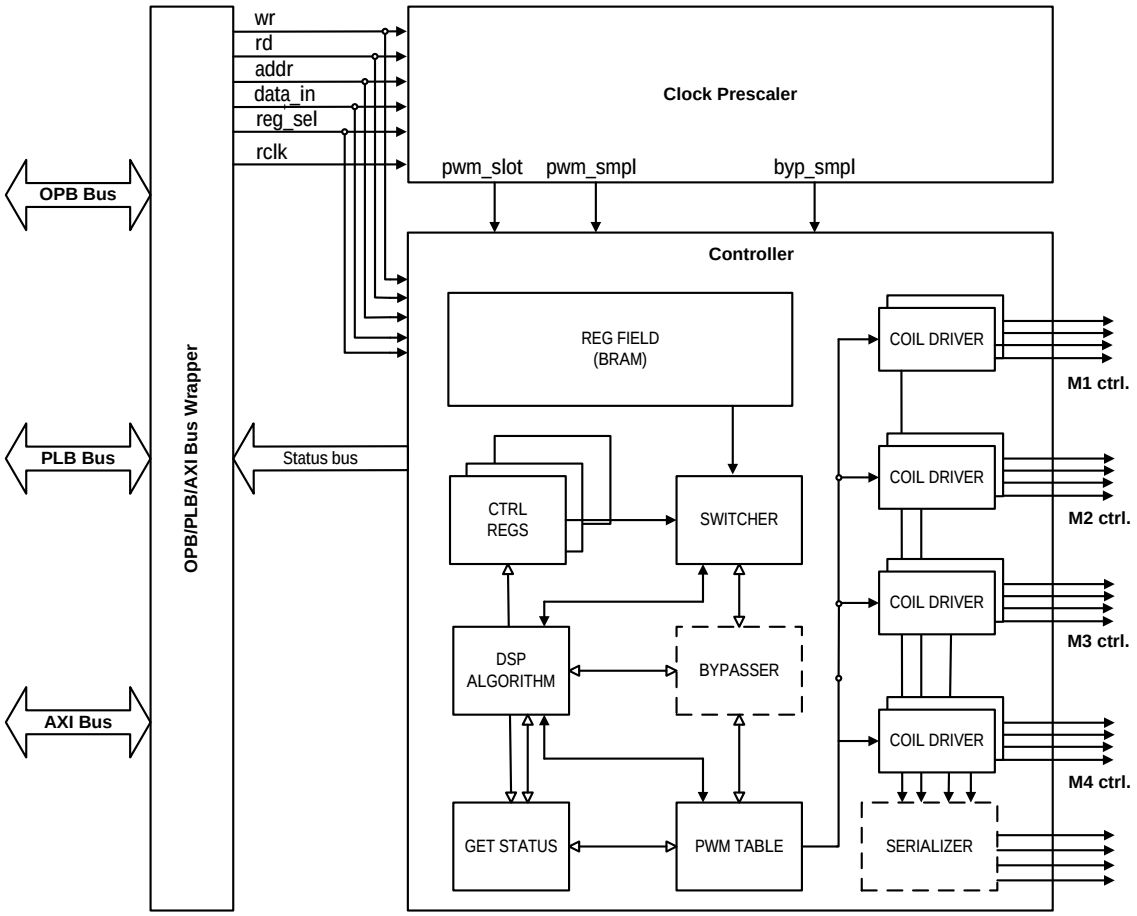

Figure 1: logiSTEP Architecture

- Low consumption of FPGA resources. Multiple IP instances can drive more than 16 motors from a single FPGA device

Applications

- Car Instrument Cluster
- Medical Equipment
- Military Applications
- Industrial Applications

General Description

The logiSTEP is a stepper motor controller IP core from Xylon's IP library logicBRICKS™. The IP supports different two-phase stepper motor driving methods: full-step, half-step and microstepping. Supported motor types are MMT and Switec X25 motors. The logiSTEP is being primarily designed for the Xilinx SoC and FPGA devices and for the automotive market. A typical example of the logiSTEP application is an automotive instrument panel (cluster).

A typical logiSTEP application puts high requirements on precise and smooth motors control. The logiSTEP IP fulfils them by hardware implemented acceleration/deceleration/smoothing algorithms. The core can be SW adjusted in different ways to assure optimal motor control.

The logiSTEP can independently drive 1 - 16 stepper motors at once. A number of motors controllable by a single FPGA device can be expanded by additional logiSTEP instances. The parameterizable VHDL design allows for customizations and IP users can control the IP core's size and features set through the implementation tools GUI.For example, the logiSTEP configured to control 4 motors uses less programmable logic than the IP instance configured to control i.e. 14 motors.

Typical motor application requires high driving currents and use of FPGA external driving circuitry. An optional logiSTEP outputs serializer can reduce a number of the requested FPGA pins in applications utilizing many stepper motors.

The logiSTEP can support the Zero Positioning Detection used for a setting up motor's rotor into a known initial position. Sensorless motion detection must be monitored by an external device interfacing the logiSTEP. Please check up the Xylon's logiHAC system for more details about the Zero Positioning Detection, or contact Xylon at support@logicbricks.com.

Functional Description

The logiSTEP internal structure is shown by the block diagram (Figure 1)

The logiSTEP's functional blocks are: Clock Prescaler, Registers module, Switcher, DSP Module, Bypasser, GetStatus Module, Serializer, PWM Table and the Coil Drivers.

Clock Prescaler

The logiSTEP IP is a fully synchronous digital design. All events within the IP happen synchronously to the bus clock signal. The Clock Prescaler module generates various clock enable signals used as different sampling signals.

Registers Module

The Registers Module includes all registers required for motor control. It combines registers implemented by BRAM and CLB logic resources. The logiSTEP uses only five registers per motor.

Switcher

The Switcher module controls internal multiplex of separated motor control channels. The logiSTEP uses large portions of the design for common tasks as presented by the block diagram.

DSP Module

The DSP Module controls motors' speed and movement precision. This logic precisely and independently defines Acceleration, Deceleration, and Smoothing control for each stepper motor control channel.

Bypasser

The Bypasser Module avoids the DSP module and directly drives motor in either clock-wise or counterclockwise direction. The movement is linear and there is no 'S-shaped' acceleration/deceleration curve. Each motor control channel can be separately programmed for either the bypass or the DSP mode of operation.

GetStatus Module

The GetStatus Module monitors current motors' positions and continuously compares them with the preset target positions. The final positioning sets up dedicated status bits that can be monitored (read) by the system's CPU.

Serializer Module

The Serializer Module takes processed motors control signals and shifts them out in serial data streams. A single pin can fully interface 2 motors, and it allows significant pinout reductions.

PWM Table

The programmable PWM Table holds various PWM values applied to produce Sine wave-like outputs at motor coils' ends. A single table supporting all controller channels is being implemented by a single BlockRAM instance. Different stepper motor models require different number of microsteps per electrical revolution and have torque vector diagrams which are not equally spaced in relation to the applied PWM controls. This is also

happening due to mechanical reasons (internal gear train, etc.), and not only due to electrical reasons. Therefore it is necessary to tailor the output PWM characteristics for each particular motor type in order to achieve the best possible precision, holding torque and smoothness for the selected motors' types. The PWM Table can store 8 CPU-programmable different PWM characteristics at once.

Coil Drivers

Motors coils must be energized in a proper order to create electromagnetic fields powering motor's rotor. Applied voltages change in time (sine wave) and generate current running in both directions through the coil. The logiSTEP IP implements digital motor coil drivers approximating ideal waveforms by PWM signals.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with Xilinx Vivado IPI and ISE Platform Studio. Many logiSTEP configuration parameters are selectable prior to the VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiSTEP VHDL configuration parameters

Parameter	Description
C_REGS_INTERFACE	CPU interface (OPB, PLB or AXI4-Lite)
C_REGS_BASEADDR	logiSTEP base address
C_REGS_HIGHADDR	logiSTEP high address
C_FAMILY	Selected Xilinx FPGA family
MOTORS_NO	Maximum number of motor controller channels
uSTEP_MAX	Maximum number of microsteps supported by motor controller channels
FRAC_CONST	The bit width of constants' fractional representation
PWM_PRESCAL_WIDTH	The bit width of prescaler defining period of output PWM's tick
BYP_PRESCAL_WIDTH	The bit width of prescaler defining duration of full-steps
SKIP_ADDR	The depth of PWM characteristics number 2 and 3
SKIP	Includes or excludes logic for usage of special PWM characteristics (No 2 and 3)
EN_BYPASS	Includes or excludes Bypass logic from the IP
EN_SER	Includes or excludes outputs Serializer
STATUS_CHECK	Includes or excludes Bypass target match control.
SER_PRESCAL_WIDTH	The bit width of prescaler defining SFT_CLK period

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Bus Interface		
PLB bus	Input/Output	PLB bus signals
OPB bus	Input/Output	OPB bus signals
AXI4-Lite Bus	Input/Output	Refer to AMBA AXI version 4 specification from ARM

Signal	Signal Direction	Description
Motors Interface		
coils_out[(MOTORS_NO*4)–1:0]	Output	Motors coils driving outputs (if serializer is used, can be left opened): A_P, A_N – first coil's controls B_P, B_N – second coil's controls coils_out[3:0] drive Motor 1, coils_out[7:4] drive Motor 2, etc. coils_out(60,56,52,48,44,40,36,32,28,24,20,16,12, 8,4,0) – A_P coils_out(61,57,53,49,45,41,37,33,29,25,21,17,13, 9,5,1) – A_N coils_out(62,58,54,50,46,42,38,34,30,26,22,18,14,10,6,2) – B_P coils_out(63,59,55,51,47,43,39,35,31,27,23,19,15,11,7,3) – B_N
zdt[(MOTORS_NO – 1):0]	Input	Recognized Zero Position Detection (ZPD) by an external logic. An input status flag into the logiSTEP.
active_mot(3:0)	Output	Selects motor for the ZPD measurements.
threestate	Output	Control flag enabling an external motor drivers' three state control for the ZPD.
out_en[(MOTORS_NO – 1):0]	Output	Control flags signalizing enabled motors.
invert_outs[(MOTORS_NO – 1):0]	Output	Control flags signalizing inverted outputs for the particular motor.
bypass_en[(MOTORS_NO – 1):0]	Output	Control flags signalizing the bypass mode for the particular motor.
sync	Output	Sync signal for synchronization with external logics.
sft_clk	Output	Shift clock output from the Serializer. This clock should be used for shifting-ion the sft_out data into an external de-ser device
strober	Output	Output strobe (latch) signal from the Serializer. This latch signal should be used for latching de-serialized data from the de-ser device into a hold device.
sft_out[((MOTORS_NO + 1)/2) – 1 : 0]	Output	Serialized outputs of the logiSTEP. Two motor channels' data are shifted out through a single logiSTEP output sft_out (0) Motor2 and Motor 1 data, sft_out(1) Motor 3 and Motor 4 data, etc.

Verification Methods

The logiSTEP is fully supported Xilinx Vivado IP Integrator and Xilinx Platform Studio integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiSTEP implementation does not require any particular skills beyond general Xilinx tools knowledge. The ISE compatible version of the encrypted IP is shipped with the compiled simulation libraries for Mentor Graphics' ModelSim. For information about Vivado compatible IP core simulations, please contact Xylon.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiSTEP IP core has been extensively used in different electronics systems, including the Xylon logiHAC Automotive Hybrid Cluster Demo. To learn more about this IP core's usage scenario, please read the application note:

URL: http://www.logicbricks.com/Documentation/App-Notes/app0038.pdf

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.00.	15.07.2009	Initial Xylon release – new doc template
2.01.	05.11.2009.	Added PLB interface and new generics
2.02.	23.11.2009.	Added new example implementation statistics table
2.03.	10.07.2010.	New doc template and implementation statistics table
3.02.	10.09.2014.	Added AXI4-Lite interface, new generic and implementation statistics table