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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	User's Manual .xdc examples
Verification	Simulated and HW validated
Reference Designs & Application Notes	
Additional Items	Bare-metal SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 AP SoC, Zynq UltraScale+™ MPSoC and all Xilinx FPGAs
- Single full-duplex asynchronous channel
- Max 1024-byte (max 512 if RX_STATUS FIFO in use) TX FIFO
- Max 1024-byte (max 512 if RX_STATUS FIFO in use) RX FIFO
- Max 512-byte receiver's status FIFO
- Baud rates from 5 bps up to > 3 Mbps
- Readable FIFO levels ("water levels")
- Flexible clock prescaler
- Software channel reset
- Independent RX and TX FIFO pointer reset
- Software driven TX signal - "break" signal for the automotive Local Interconnect Network (LIN) protocol
- Framing error detection, parity error detection and "break" error detection (for LIN protocol)
- Automated flow control or software flow control using CTS and RTS control signals
- Programmable trigger levels for receiver and transmitter FIFO interrupts and automatic flow control
- Transmitter idle interrupt (shift register and FIFO both empty)
- Receiver's timeout interrupt
- Programmable data length (5, 6, 7, 8)
- Programmable number of stop bits (1, 1.5, 2)
- Programmable parity type: none, even, odd, space and mark
- Modem control functions (DSR, DTR, DSR, DCD and RI)

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) clk	LUT[1]	FF[1]	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z020-1)	170	323	337	2	0	0.5	0	0	N/A	Vivado 2018.3
Zynq® UltraScale+ (XCZU9EG-1)	250	316	337	2	0	0.5	0	0	N/A	Vivado 2018.3

Notes:
1) Assuming the following configuration: 256 bytes deep RX FIFO, 256 bytes deep TX FIFO, 32-bit AXI4-Lite register interface.
2) Assuming only register interface connected internally, RX and TX routed off-chip, handshake and modem control signals not used.

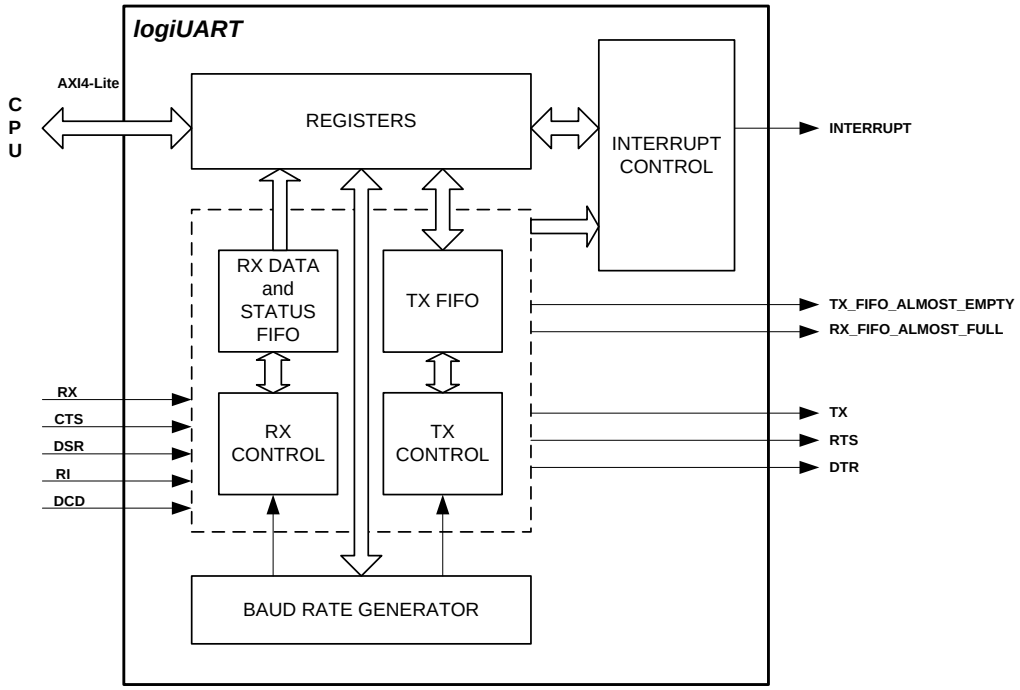

Figure 1: logiUART Architecture

Features (Cont)

- TX FIFO and RX FIFO status accessible through logiUART ports, which is useful for an external Direct Memory Access (DMA) Controller
- Register access interface compliant to the ARM® AMBA® AXI4-Lite interface specification
- Can be tailored to fulfill your need
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Vivado® and ISE® Design Suits*

** The last logiUART IP core version for the Xilinx ISE Design Suite: v2_02_a*

Applications

- Automotive systems – LIN support
- Serial data communications in SoCs

General Description

The logiUART is a single-channel programmable UART, which enables automotive Electronic Control Units (ECUs) to communicate within the vehicle's body through the Local Interconnect Network (LIN). In order to support the LIN protocol, the logiUART IP core implements an optionally software driven TX signal – "break" signal, as well as the "break" error detection. Due to the small IP core's size, even the smallest FPGA devices can accommodate multiple LIN network nodes by using multiple logiUART instances.

The logiUART offers simplicity in use and high overall performances. Communication speeds are supported in a wide range, starting from a few bps and up to more than 3 Mbps. The 1024-bytes deep TX and RX FIFOs reduce the CPU overhead and the readable FIFOs' pointers with supported interrupts enable flexible software control. The IP core supports various character formats, as well as different types of parity protection and framing errors. The logiUART is configured and delivered with the standard bus interfaces that enable easy interfacing with soft-core and hard-core CPUs in Xilinx All Programmable devices.

The logiUART is a real plug-and-play IP core, supported by the Xilinx Vivado Design Suite, and designers familiar with the toolset can immediately start designing. The IP's size and features can be easily adjusted through IP drag and drop Vivado graphical user interface (GUI).

Functional Description

The logiUART core consists of: internal Registers with Interrupt Control logic, Baud Rate Generator, as well as TX and RX Blocks featuring FIFOs. The internal structure is shown in the block diagram – Figure 1.

Registers

All internal registers used for control and data exchange with the CPU are implemented in Registers module and are accessible through the AXI4-Lite bus.

Interrupt Controller

The interrupt controller generates interrupt signals for the CPU; if interrupt conditions are satisfied and particular interrupts are enabled. Interrupts depend on FIFOs' states and receive and transmit data.

Baud Rate Generator

TX and RX FIFOs' control and shift registers are paced by a baud rate clock generated by programmable 20-bit baud rate counter. Every RX bit is sampled several times (oversampling) and the number of samples per bit is programmable.

TX and RX Control Logic with FIFOs

The TX and the RX FIFOs' depths are configurable: from 16 up to 1024 bytes. The FIFOs are real dual-port FIFOs, implemented in Xilinx Block RAMs (BRAMs). One port is used for CPU accesses and the other one for the TX or the RX control logic. The transmitter pops characters from the top of the TX FIFO and passes them to the TX shift register. It also takes care of FIFO statuses (empty, full), implements the TX parity calculation and checks the "water level" as well. The receiver filters input characters and passes them into a shift register that pushes the completed characters onto the RX FIFO's top. The RX control logic takes care of FIFO statuses (empty, full). RX parity check, framing check and water level check are also done in this module.

Core Modifications

The core is supplied in an encrypted VHDL format which allows the user to take a full control over configuration parameters. Table 2 outlines the most important logiUART configuration parameters selectable prior to the VHDL synthesis. For a complete list of parameters, please consult the User's Manual delivered with the IP core.

Table 2: logiUART VHDL configuration parameters

Parameter	Description
C_USE_RX_STAT	Enable/disable usage of RX data status FIFO
C_TX_FIFO_DEPTH	Determines the size of logiUART TX FIFO
C_RX_FIFO_DEPTH	Determines the size of logiUART RX FIFO
C_BAUDRATE_REG	The initial value of the baudrate register
C_FORMAT_REG	The initial value of the format register
C_SAMPLE_REG	The initial value of the sample register
C_RX_LEVEL_REG	The initial value of the RX level register
C_TX_LEVEL_REG	The initial value of the TX level register
C_RTS_LEVEL_REG	The initial value of the RTS level register
C_TIMEOUT_REG	The initial value of the timeout register

The logiUART has been designed with regard to adaptability to various applications. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiUART core or to implement some of your specific functions, you can allow us to tailor the logiUART to your requirements. The logiUART source code is available at additional cost from Xylon.

Core I/O Signals

The core signals I/O have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal name	Signal Direction	Description
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to AMBA AXI version 4 specification for ARM
Serial interface signals		
RX	I	Received serial data
TX	O	Transmitted serial data
CTS	I	Clear To Send serial control signal
RTS	O	Request To Send serial control signal
DTR	O	Data Terminal Ready serial control signal
DSR	I	Data Set Ready serial control signal
RI	I	Ring Indicator serial control signal
DCD	I	Data Carrier Detect serial control signal
DMA		
TX_FIFO_ALMOST_EMPTY	O	TX FIFO almost empty
RX_FIFO_ALMOST_FULL	O	RX FIFO almost full
Interrupts		
INTERRUPT	O	Interrupt signal, level sensitive, high active

Verification Methods

The logiUART is fully supported by the Xilinx Vivado (IPI) and ISE (XPS) Design Suits. This tight integration tremendously shortens IP integration and verification. A full logiUART implementation does not require any particular skills beyond general Xilinx tools knowledge. For information about Vivado compatible IP core simulations, please contact Xylon.

The logiUART evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

http://www.logicbricks.com/Products/logiUART.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx Vivado Design Suite
- ModelSim

Available Support Products

To learn more about the Xylon logicBRICKS IP cores and development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.01	04.03.2009	Initial Xylon release – new doc template
1.07	06.04.2010	PLBv46/OPB register interface, configurable FIFOs' depths New doc template
2.00	02.12.2010.	AXI4-Lite register interface added
2.01	12.11.2012.	Added register interface byte swap option
2.02	25.02.2015	Document version updated according to the IP core Updated Table 1
2.3	26.01.2017	Document version updated according to the IP core Updated Table 1, Table 2 and Table3, Figure 1. Added support for MPSoC, ZYNQ and Vivado tool. Removed OPB and PLB bus interfaces. Removed logiCRAFT-CC.
2.4	20.02.2019	Updated Table 1.