Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Verification	Reference design simulation
Reference Designs & Application Notes	Vivado reference design
Additional Items	SW drivers, API and post-processing library
Simulation Tool Used	
Vivado Simulator	
Support	
Support provided by Xylon	

Features

- Advanced object classification core for support of Vehicle Detection in camera-based video systems
- Algorithm based on a cascade of weak classifiers using Local Binary Pattern (LBP) features
- Trained for car and truck recognition on wide range of automotive scenarios
- Run-time variable image size
- Supports resolutions up to 4096x4096
- Support for multiple scale detection
- Template size 24x24 pixels
- Run-time variable window shift
- Supports Xilinx® Zynq®-7000 and Zynq®-UltraScale+ SoC All Programmable SoC
- ARM® AMBA® AXI4 compliant Memory Mapped Register Interface
- AXI4 Slave Stream Video Input Interface
- Support RGB and YUV video stream format
- High Input Data rate (> 150 Mpixels per Second)
- High Throughput (> 64 GOP/sec)
- Frame rate of 25 fps with multiple scales
- Detection range from 5 to 100 m
- Simple programming due to a small number of control registers
- Vivado® reference design including demo software application
- C code API and post-processing library available

Applications

- Driving Assistance Systems such as Adaptive Cruise Control and Forward Collision Warning
- Content Based Indexing
- Traffic Monitoring

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) [1] sysgen_clk	LUTs[2]	FFs[2]	IOB	CMT	BRAM[3]	DSP48A	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z045-2)	250	6,408	4,285	0	0	33.5	0	0	N/A	VIVADO® 2017.4
Zynq®-UltraScale+ (XCZU9EG-2)	300	6,375	4,282	0	0	33.5	0	0	N/A	VIVADO® 2017.4

Notes:
1) The maximum pixel rate is half Fmax
2) Including AXI4-lite interface and assuming configuration with default IP parameters, max image size = 1024x1024, max template size = 24x24
3) Number of RAMB36

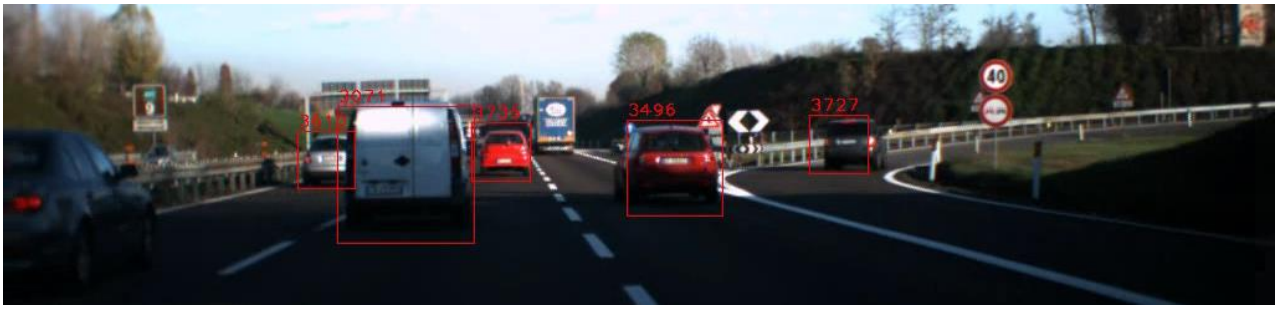

Figure 1: Vehicle Detection – Screenshot

General Description

The logiVDET is a learning-based vehicle detection IP core, developed for vision-based embedded applications, from the Xylon logicBRICKS IP core library. The algorithm follows a discriminative approach based on a cascaded classifier using Local Binary Pattern features. This architecture makes the detection process faster rejecting the negative examples in the initial stages of the cascade, while the computation effort is mainly spent on the templates hard to classify.

Local Binary Pattern (LBP) is a very efficient texture operator which labels the pixels of an image by thresholding the neighborhood of each pixel and considers the result as a binary number. The most important property of the LBP operator in real-world applications is its robustness to monotonic gray-scale changes caused, for example, by illumination variations. Another important property is its computational simplicity, which makes it possible to analyze images in challenging real-time settings. LBP is being used as an alternative to Haar-like features in many domains.

The classifier was trained to recognize wide variety of rear views of cars and trucks on the basis of a wide training set of examples (Figure 2).

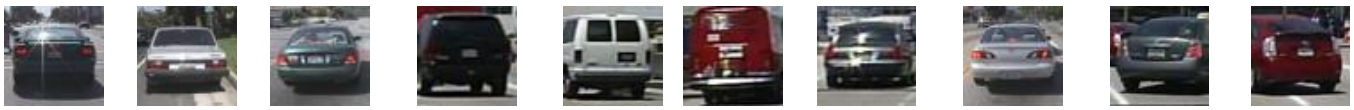

Figure 2: Example of vehicles used for the training set

The core itself works at a single scale, i.e. it recognizes vehicles at a fixed size. Extension to multiple scales is given by inserting the core in a framework that provides it with a sequence of re-scaled versions of the same input frame. This way, it is possible to detect vehicles in an arbitrary range of distances. For example, with 20 levels of scale (1 MPixel camera with 50 degrees of lens FOV) it is possible to detect vehicles in a range from 5 to 100 m running at 30 fps.

logiVDET is fully AXI4 compliant and supports Xilinx Zynq -7000 All Programmable SoC.

The IP core is provided with C code API and software library implementing post-processing task such as groping, tracking, distance estimation, and vehicle overlay. Calibration utilities are also available.

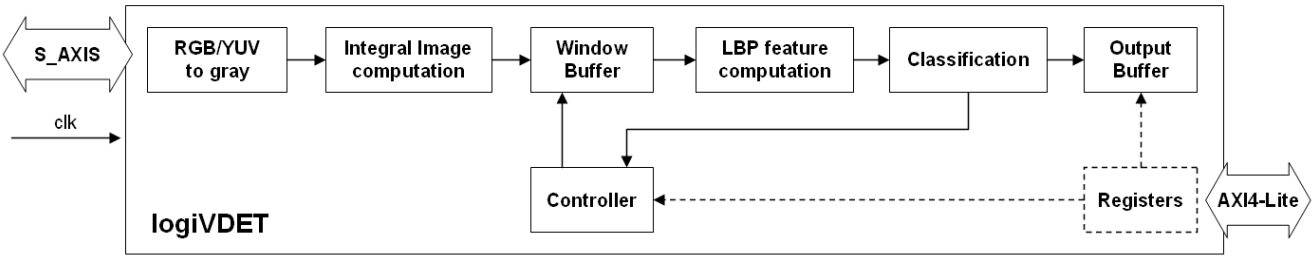

Figure 3: logiVDET Architecture

Functional Description

The Figure 3 presents internal logiVDET IP core's architecture. The logiVDET functional blocks are: RGB/YUV to Gray, Integral Image Computation, Controller, Window Buffer, LBP Feature Computation, Classification, Output Buffer and Registers.

RGB/YUV to Gray block

This optional block converts the input video stream from YUV4xx or 24-bit RGB888 format to Y8-bit (gray levels).

Integral Image Computation block

The Integral Image (or Summed Area Table) is used as a quick and effective way of calculating the sum of pixel values in a given rectangular region of the given image. Once the Integral Image is computed, you can calculate the summed area of any rectangular region with just few additions.

Controller block

This block is responsible of the overall execution flow. A FSM rules about the classification progress, the detection window sliding and the AXI4 Stream handshaking, on the basis of the results of the classification.

Window Buffer block

This block is used for buffering (in block rams) the Integral Image. The buffer is sequentially written and randomly read in order to calculate the summed areas necessary to the LBP feature computation.

LBP Feature Computation block

This block is responsible of the LBP feature computation. Three LBP feature computation engines works in parallel to maximize the throughput. Three features can be computed at each pixel clock cycle.

Classification block

For each stage this block checks the membership of the LBP features to the subsets, accumulates the weights and determins the prosecution of the classification process to the next stage.

Output Buffer block

This block queues in the buffer the detected vehicle coordinates. For each detection the scale index and the (x,y) position are memorized in the output buffer for each detection. At the end of the processing of all the scales of the sequence a flag is asserted in order to alert the CPU that the results are ready to be read out.

Registers block

The register interface can be configured as AXI4-Lite interface.

IP Configuration and Performances

The classifier parameters coming from the training, as well as the maximum size of the input image, can be updated at compilation time. The length of the scale sequence, the sizes of the ROIs, and the step of the detection window at each scale can be programmed in software run-time.

With the default configuration (related to the FPGA resource occupation in Table 1) we have 20 stages, 555 weak classifiers, a template size of 24x24 pixels and a maximum image width of 1024 pixels. With scale sequence of 18 ROIs, 1 MPixel camera and a 50 degrees of FOV lens, it is possible to detect vehicles in a range from 5 to 100 m at a frame rate of 30 fps.

Software library

logiVDET IP core is provided with a software C code library optimized for Zynq 7000 including post processing functions such as vehicle grouping, vehicle tracking, vehicle distance estimation, diagnostic, vehicle overlay and display management. Software utilities for system calibration, configuration and PC-based emulation are also provided.

Core I/O Signals

Descriptions of all signals I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk	Input	input processing clock
AXI4-Stream signals (slave bus)		
s_axis_tdata(23:0)	Input	Video Data: • for 24-bit RGB input (RED [23:16] ; GREEN [15:8] ; BLUE [7:0]) • for 16-bit YUV422 input type only 15:0 is in use (U/V [15:8] ;Y [7:0])
s_axis_tvalid	Input	Valid
s_axis_tuser	Input	Start Of Frame
s_axis_tlast	Input	End Of Line
s_axis_tready	Output	Ready
Register Interface		
AXI4-Lite Interface	BUS	Refer to AMBA AXI version 4 specification from ARM

Verification Methods

The logiVDET IP core is fully supported by Xilinx Vivado design tool. This tight integration tremendously shortens IP integration and verification. A full logiVDET implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Xilinx System Generator for DSP (MathWorks Matlab/Simulink) to source model access

Available Support Products

The logiVDET IP core can be evaluated on the logiADAK Advanced Driver Assistance (ADAS) Development Kits that allow customers to fully evaluate performance on their vehicle or in the laboratory.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: https://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00.a	03.01.2014	Initial datasheet release
2.0.1	24.11.2014	Vivado release
2.0.2	27.03.2015	Minor changes
2.0.3	28.08.2018	Implemented on Xilinx Zynq UltraScale+

The logiVDET core is sourced from Technology Partner
eVS embedded Vision Systems Srl.