## Xylon d.o.o.

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## Core Facts

| Provided with Core | |
|---|---|
| Documentation | User's Manual |
| Design File Formats | Encrypted VHDL |
| Constraints Files | Reference designs constraint files |
| Reference Designs & Application Notes | Xilinx Vivado® IP Integrator reference design available with the logiADAK kit |
| Additional Items | - Linux SW driver, helper library, mathematical library<br>- logiADAK Automotive Development Kit (provided separately) |
| **Simulation Tool Used** | |
| Mentor Graphics' Modelsim | |
| **Support** | |
| Support provided by Xylon | |

## Features

- Supports Xilinx® Zynq®-7000 SoC and Zynq UltraScale+™ MPSoC programmable devices
- For information about FPGA support, please contact Xylon
- Supports arbitrary video transformations defined by MLUTs (Memory Look Up Table):
  - video texturing on curved planes (non-linear)
  - arbitrary combination of homographic transformations; rotating, translating, cropping, perspective changes…
- Enables the virtual flying camera feature
- Equalizes colors within the multi-camera system under changing illumination conditions
- Supports corrections of fisheye lens distortions
- Suitable for video systems with extreme wide-angle lenses (fisheye) with Field Of View (FOV) up to 180º
- High performance, e.g. up to 140 MPix/s in 150 MHz operating systems
- Supports up to 2048 x 2048 input and output resolutions; 60 fps and higher frame rates
- Higher video input resolutions and frame rates can be supported by multiple IP instances that work in parallel
- Configurable number of video inputs (up to 8) and video outputs (up to 8)
- Supports square and non-square pixels (pixel aspect ratio) at the video input
- IP deliverables include a Linux user space driver, Xylon's mathematical library and helper library
- Xylon's advanced logiADAK Builder PC software enables easy IP configuration within Xylon's ViewMore™ Natural Surround View ADAS SoC solutions
- Tile rendering for improved performance and efficiency

**Table 1: Example Implementation Statistics for Xilinx® SoC/FPGAs**

| Family (Device) | Fmax (MHz) | LUT[1] | FF[1] | IOB[2] | BRAM Tile | DSP | PLL/ MMCM | BUFG/ BUFR | GTx | Design Tools |
|---|---|---|---|---|---|---|---|---|---|---|
| Zynq UltraScale+ (xczu9eg-ffvb1156-2-e) | 200 | 14310 | 13144 | 0 | 46.5 | 86 | 0 | 0 | 0 | Vivado 2019.2 |

1) Assuming the Automotive Surround View Driver Assistance (DA) system's configuration: 6 input cameras, 32-bit AXI-Lite register interface, 64-bit AXI memory interface for LC, MLUT and MLUT_LVL, 128-bit AXI memory interface for TC and OB, lens correction, YUV color space on input and RGB color space on output, 2k input and output resolution

2) Assuming register and memory interfaces are connected internally

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- Supports input/output color spaces: RGB/RGB, YCbCr(4:2:2)/YCbCr(4:2:2) and YCbCr(4:2:2)/RGB
- Independent double/triple buffering for up to 8 asynchronous video inputs
- Independent double/triple buffering for up to 8 asynchronous video outputs
- Simple programming of control registers through the ARM® AMBA® AXI4-Lite interface
- Video memory interface type: AMBA AXI4
- Prepared for the Xilinx Vivado® Design Suite 2019.2 and newer versions of implementation tools
- Parametrical VHDL design that allows tuning of features set and consumption of FPGA resources
- Simple Plug'n'Play of other Xylon logicBRICKS IP cores, such as the logiWIN frame grabber, logiCVC-ML display controller and logiISP-UHD HDR Image Signal Processing (ISP) Pipeline

## Applications

- Automotive Advanced Driver Assistance Systems (ADAS): Surround View, Pedestrian Detection, Lane Departure Warning, Rear-View Camera, Heads-Up Display (HUD)…
- Industrial systems: Surveillance Systems such as the Multi-Head 360° Panoramic Wide Camera with no blind spots, Industrial Pipe Inspection equipment, Test equipment…
- Medical endoscopy and similar equipment
- Defense video and vision systems, e.g. smart helmets, panoramic turret cameras, etc.

## General Description

The logiVIEW Multiview 3D Video Transformation Engine is Xylon's logicBRICKS IP core optimized for Xilinx' Zynq-7000 SoC, Zynq UltraScale+ MPSoC and newer FPGAs. It is designed for high-performance and real-time processing of multiple video streams or still images. The logiVIEW IP core removes fisheye distortions caused by extreme wide-angle Field Of View (FOV) lenses, and makes perspective corrections and other homographic transformations (Figure 1) to the captured video. It can also execute complex arbitrary non-homographic transformations, such as video texturing on curved planes (Figure 2), defined by MLUTs (Memory Look-up Table). MLUT transformations are key logiVIEW IP core's features for 3D Surround View parking assistance ADAS applications (Figure 3). Multiple processed video or still image outputs can be stitched together, resulting in a high-definition video output image. Stitching and blending between multiple video streams is done within the logiVIEW IP core without the need for external IPs.

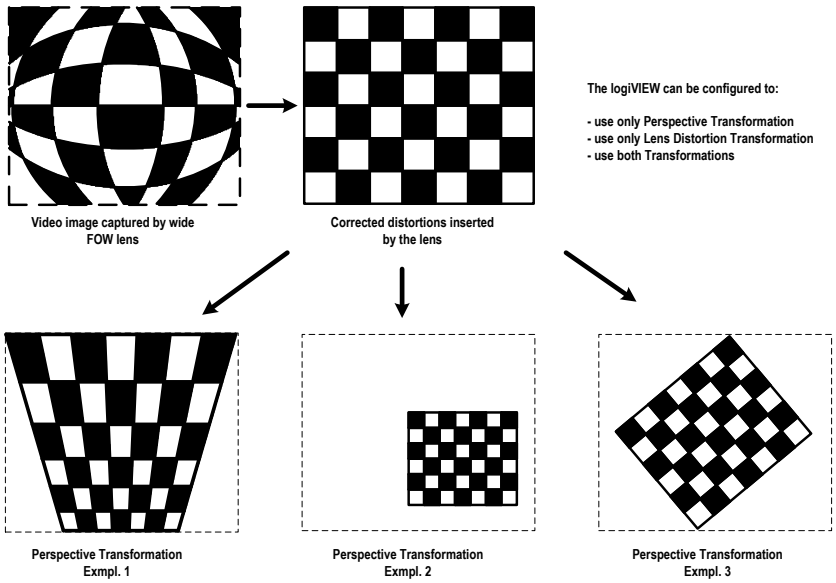


**Figure 1: Homographic Transformations Examples**

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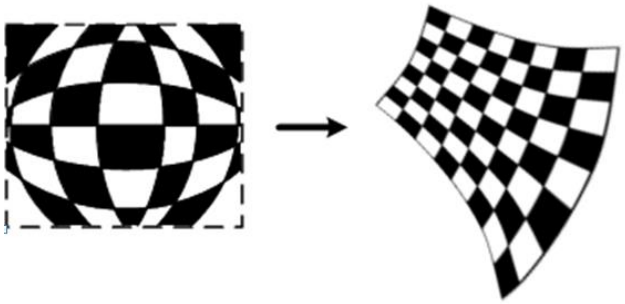

**Figure 2: Example MLUT Transformation**

The logiVIEW IP core is used in automotive ADAS applications, such as the Multi-Camera System for Surround View parking assistance, Heads-Up Displays (HUD), Lane Departure Warning, Rear-View (Back-Up) and others. Due to its high versatility and configurability, it can also be used in many other non-automotive, single or multi-camera applications, such as medical endoscopy, surveillance and defense systems (Panoramic 360° View camera - Figure 4), etc.

The logiVIEW is a highly configurable IP core. Xilinx' implementation tools enable easy tuning of the logiVIEW's consumption of programmable logic resources and the features set set up through an easy-to-use GUI interface. Table 2 shows a small excerpt of the configuration parameters list that can be set up prior to the core's synthesis time. IP configurations which utilize only the lens transformation or the MLUT transformation are good examples of balancing between the required features set and used programmable logic resources.

The logiVIEW IP core can handle up to eight video inputs and video outputs, as long as the system architecture allows it. The available memory bandwidth, frame rates of input video cameras, and other system parameters determine the number of supported video inputs and outputs by a single logiVIEW IP core.

For example, the YCbCr 422 video format requires lower memory bandwidth than the RGB video format, and the logiVIEW IP core instance configured to use the YCbCr pixel format can support more video channels and higher video resolutions with the same memory controller subsystem (SoC bus and memory controller IP core), and the memory device(s) connected to the FPGA. Video format can be set up through the IP core's configuration GUI interface.

In video applications that require more processing power than offered by a single logiVIEW IP core instance, it is possible to implement parallel processing of video inputs' segments by multiple logiVIEW IP core instances and to achieve application goals.

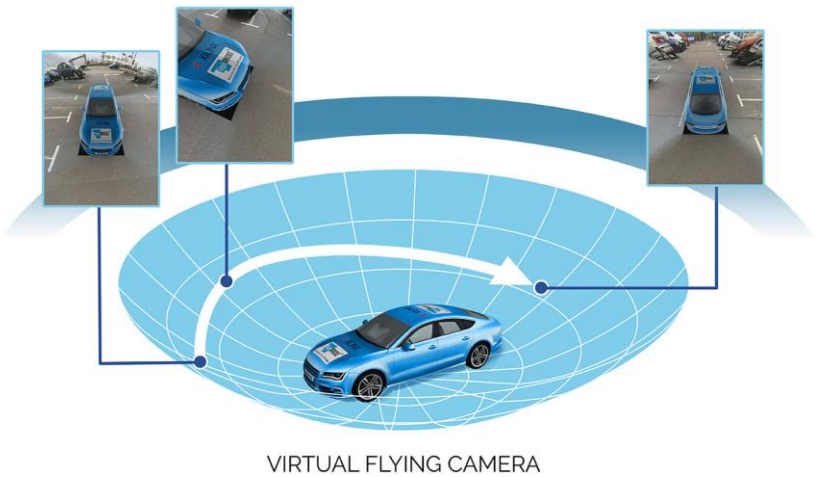


**Figure 3: Dynamically changeable 3D views generated by the logiVIEW IP Core**

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**logiVIEW Application - Automotive Surround View Driver Parking Assistance**

The Surround View driver parking assistance (Figure 3) provides an unmatched awareness of the situation by enabling the driver to see 360-degrees around the vehicle on the LCD instrument cluster or the Central Information Display (CID). The system uses at least 4 cameras, furnished by extreme wide-angle fisheye lenses, which cover separated zones around the vehicle. The logiVIEW IP core must remove the lens distortions, correct perspectives to four high-resolution input video streams, and stitch the corrected video images in a single display of the vehicle's surroundings.

Xylon's ViewMore Natural Surround View solution, which is based on the logiVIEW IP core, enables drivers to dynamically adjust the position of the virtual flying camera and to see the vehicle's naturally looking surroundings in a three-dimensional hemispheric view displayed in fine-detail HD resolution. This complete ADAS solution is presently used on the road in production automotive systems. The solution can be fully evaluated on Xilinx' Zynq UltraScale+ AP SoC based logiADAK Automotive Driver Assistance Development Kit.

To learn more about Xylon's Surround View ADAS, please visit:
http://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit.aspx

**logiVIEW Application – Multi-Head 360° Video Camera for Surveillance Applications**

A video surveillance multi-head camera with no blind spots that shows a 360° view (Panoramic View) of the surroundings isanother example of the logiVIEW IP core's application. The camera setup can use, for example two, three or more video cameras with wide angle lenses to cover the full perimeter around the protected object. To support this type of applications, the logiVIEW IP core must be programmed by software in a different way than the previous application example.

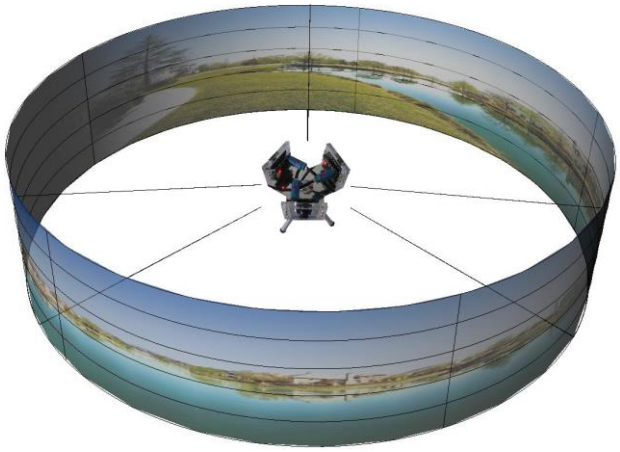

**Figure 4: Panoramic View Camera Example**

## Core Modifications

The logiVIEW IP core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator tool. Different logiVIEW configuration parameters are selectable prior to VHDL synthesis, and the below table presents a selection from a list of available configuration parameters. The logiVIEW is designed with regard to adaptability to various SoC designs.

However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiVIEW core in your specific implementation or to supplement some of your specific functions, you can allow us to tailor the logiVIEW to your requirements.

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**Table 2: logiVIEW VHDL configuration parameters**

| Parameter | Description |
|---|---|
| C_USE_LT | Use the Lens Transformation block |
| C_USE_MLUT | Use the Memory Look-up Table block |
| C_USE_MCD | Use the Misscalibration detection block |
| C_USE_COLOR_EQU | Use the Color equalization statistic block |
| C_USE_GAIN | Use the Color equalization gain block |
| C_USE_IN_BUFF | Enables input image's buffering to prevent video flickering. |
| C_USE_OUT_BUFF | Enables output image's buffering to prevent video flickering. |
| C_PIX_IN_FORMAT | Use RGB, YCbCr (4:4:4) , YCbCr (4:2:2) or Luma only input format |
| C_PIX_OUT_FORMAT | Use RGB, YCbCr (4:4:4) , YCbCr (4:2:2) or Luma only output format |
| C_CAMERA_NUM | Number of input cameras |

## Core I/O Signals

The core's I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

**Table 3: Core I/O Signals**

| Signal | Signal Direction | Description |
|---|---|---|
| **Global Signals** | | |
| RST | Input | Global synchronous set/reset |
| CLK | Input | Memory clock |
| **Memory Interface** | | |
| AXI4 Interface | Bus | Refer to AMBA AXI4 specifications |
| **Register Interface** | | |
| AXI4-Lite Interface | Bus | Refer to AMBA AXI4-Lite specifications |
| **Auxiliary Signals** | | |
| HW_TRIGG | Input | Hardware trigger signal for start of processing, edge sensitive, active high |
| INTERRUPT | Out | Interrupt signal, level sensitive, active high |
| VIDEO_IN_CURR_VBUFF | Input | Video input double/triple buffering: Current video memory buffer |
| VIDEO_IN_NEXT_VBUFF | Out | Video input double/triple buffering: Next video memory buffer to write to |
| VIDEO_IN_SW_VBUFF | Input | Video input double/triple buffering: Request for buffer switching |
| VIDEO_IN_SW_GRANT | Out | Video input double/triple buffering: Buffer switching granted |
| VIDEO_IN_ODD_FIELD | Input | Video input odd field, for de-interlacing |
| VIDEO_OUT_CURR_VBUFF | Out | Video output double/triple buffering: Current video memory buffer |
| VIDEO_OUT_NEXT_VBUFF | Input | Video output double/triple buffering: Next video memory buffer to write to |
| VIDEO_OUT_SW_VBUFF | Out | Video output double/triple buffering: Request for buffer switching |
| VIDEO_OUT_SW_GRANT | Input | Video output double/triple buffering: Buffer switching granted |

## Verification Methods

The logiVIEW is fully supported by the Xilinx Vivado Design Suite, which tremendously shortens IP integration and verification processes. A full logiVIEW implementation does not require any particular skills beyond general Xilinx tools knowledge.

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## Available Support Products

The logiADAK Programmable MPSoC Advanced Driver Assistance (ADAS) Kit is Xilinx' Zynq Ultrascale+ MPSoC based automotive development platform that showcases multi-camera central module processing including the production-ready "ViewMore Natural Surround View" IP solution. The logiADAK can be used to quickly bring new ADAS innovations to market. It provides ADAS designers with all the resources they need to efficiently develop vision-based ADAS systems, save months of development time, and focus efforts on system differentiating functions and performance.

To learn more about the logiADAK Automotive Driver Assistance Kit, contact Xylon or visit the following website:

Email: support@logicbricks.com
URL: www.logicbricks.com/Products/logiADAK.aspx

## Ordering Information

This product is available directly from Xylon under the terms of Xylon's IP License. Please contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com/Products/logiVIEW.aspx

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## Related Information

### Xilinx Programmable Logic

For information on Xilinx' programmable logic or development system software, contact your local Xilinx sales office or:

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## Revision History

| Version | Date | Note |
|---|---|---|
| 2.00. | 04.06.2010 | Preliminary Xylon release – new doc template |
| 2.00.e | 03.03.2011 | Changed data in Table 2. Added description of new MLUT feature and YCrCB/RGB converter. |
| 2.00.f | 01.04.2011 | First public version. Added short Calibration Software description. |
| 3.05 | 19.11.2012 | Support for bowl-shaped surface projections (3D visualization), dynamic stitching, new calibration software, and the second generation logiVIEW-SVK, updated resources |
| 3.10 | 18.03.2015 | Initial Vivado version of IP core. Support for non-swizzled texture, non-square pixel size. |
| 3.11 | 27.05.2015 | Pixel color calculation improved for YUV 4:2:2, added buffer registers and busy flag. |
| 5.2 | 18.02.2020 | Modified Tables 1, 2 and 3. Added color equalization and description of the flying camera feature. |

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