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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc examples
Reference Designs & Application Notes	Vivado® IP Integrator reference designs
Additional Items	Free reference designs for Xilinx MPSOC based Xylon's vision kits SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, Zynq® UltraScale+™ MPSoC, Versal™ ACAP and all Xilinx 7 series FPGA families
- Available Linux V4L2 and bare-metal SW drivers
- Supports parallel video input and ARM® AMBA® AXI4-Stream video input
- Support for 1, 2 and 4 pixel per clock input video
- Supports versatile digital video input formats:
  - **ITU656 and ITU1120 (PAL and NTSC)**
  - **RGB**
  - **YUV 4:2:2**
  - **YUV 4:4:4**
  - **Y (Mono)**
- Can switch between two video inputs with same or different video formats
- Maximum input resolution is 8192 x 8192 pixels, maximum output resolution is 8192 x 8192 pixels
- Configurable and programmable output row stride, maximum row stride is 8192 pixels
- Built-in YUV to RGB converter and RGB to YUV converter
- Real-time video scale-up (zoom in) up to 64x
- Real-time video scale-down (zoom out) down to 16 times

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LUT[1]	FF[1]	IOB[2]	CMT	BRAM	DSP	DCM/ CMT	GTx	Design Tools
	mclk	vclk	rclk									
Zynq-7000 (XC7Z020-1)	128	160	150	1625	1898	9	0	4	11	0	0	Vivado 2018.3
Zynq UltraScale+ (XCZU9EG-1)	240	320	220	1650	1902	9	0	4	11	0	0	Vivado 2018.3
Versal ACAP (XCVC1902-VSVA2197-1)[3]	200[4]	/	110[4]	2993	2160	0	0	6	8	0	0	Vivado 2019.2

1) Assuming the following configuration: ITU656, RGB565 output, 32-bit AXI4-Lite register interface, 64-bit AXI4 memory interface with max. burst size of 16 words, scaling in both directions with multipliers (DSP48s), programmable output stride.
2) Assuming only video input signals are routed off-chip, register and memory interfaces are connected internally.
3) logiWIN on Versal is routed with following configuration: AXI Stream YUV422, RGB888 output, 32-bit AXI4-Lite register interface, 128-bit AXI4 memory interface with max. burst size of 64 words, scaling in both directions with multipliers (DSP58s), programmable output stride.
4) axis_clk is same as mclk. Frequencies on Versal device are not expressed as maximum possible frequencies.

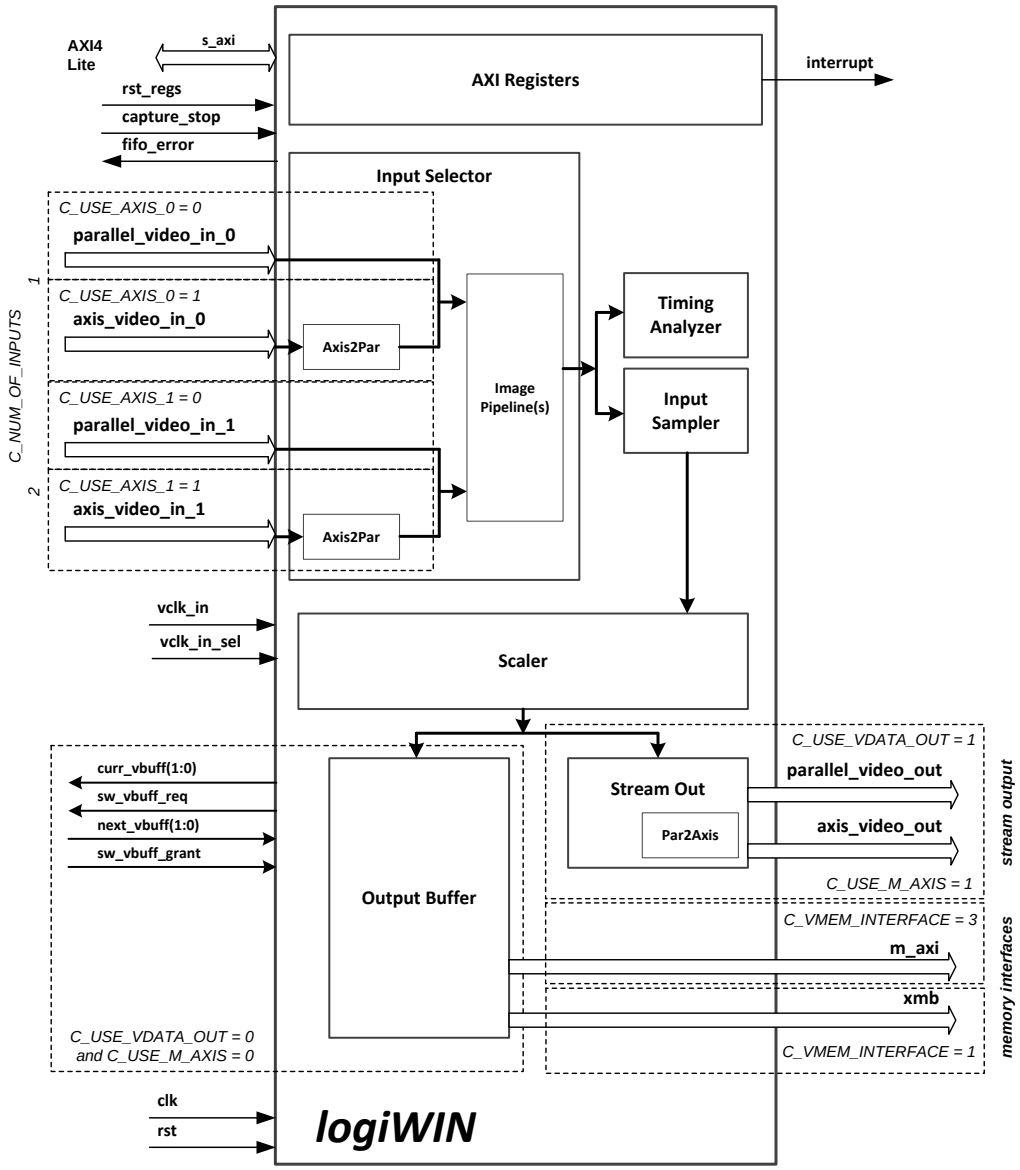

Figure 1: logiWIN Architecture

Features (cont)

- Lossless 2x scaling down or 4x in the cascade scaling mode
- Embedded image color enhancements (contrast, saturation, brightness and hue for YUV video inputs
- Supports video input cropping and smooth image positioning
- Configurable output type: video memory interface, parallel stream video output or ARM® AMBA® AXI4-Stream video output
- ARM® AMBA® AXI4 video memory interface
- Configurable ARM® AMBA® AXI4-Stream video output data width: 1, 2 or 4 pixels per clock

Features (cont)

- Supports versatile digital video output formats:
  - **RGB565, BGR565**
  - **RGB888, BGR888**
  - **ARGB6565, ABGR6565**
  - **ARGB8888, ABGR8888**
  - **YUV 4:2:2**
  - **YUV 4:4:4**
  - **Y (Mono)**
  - **TRUERGB888 (3BPP)**
  - **Planar RGB888, YUV444 and YUV422 format**
- ARM® AMBA® AXI4-Lite bus compliant register interface
- Configurable registers' default values, it allows logiWIN usage without any software initialization
- Supports pixel alpha blending – program the alpha channel in the output video stream
- Stream or stop video
- Supports Big and Little Endianness memory layout
- Supports normal and swizzle memory layout
- Double or triple buffering for flicker-free video
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Vivado® IP Integrator (IPI) implementation tools
- Free Vivado IPI for Xilinx Zynq-7000 AP SoC ZC702 Evaluation Kit
- Plug-and-Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiCVC-ML (Compact Video Controller with Multilayer Alpha Blending) and logiVIEW Perspective Transformation and Lens Correction Image Processor IP core for complex real-time video processing

Applications

- Advanced Driver Assistance and Autonomous Driving (ADAS/AD)
- Computer vision, industrial imaging, Surveillance, Test equipment and Robotics
- Medical Applications
- Aerospace and Defense systems, etc.

General Description

The logiWIN is a frame grabber and scaler IP core from the Xylon logicBRICKS IP core library optimized for Xilinx All Programmable devices. It is designed to receive video input stream, to scale it, and to give an output video formatted in several digital video formats. The logiWIN IP core functions include scaling, cropping, positioning, color and format conversions, and masking of the output image by non-rectangular masks. The interlaced PAL/NTSC input video streams can be de-interlaced. The logiWIN can be used as scaler (AXI4-Stream video output) or as frame grabber with scaler (video memory interface). The interface to the video memory is designed for SDRAM (SDR, DDR, DDR2, DDR3…) and SRAM frame buffer implementations. For easier system integration, the logiWIN uses ARM AMBA AXI4, AXI4-Stream and AXI4-Lite buses. Multiple logiWIN IP core instances enable simultaneous processing of multiple video inputs or one high resolution video input by a single Xilinx Versal ACAP, Zynq-7000 AP SoC or FPGA chip.

Standard bussing architecture, software support and IP core deliverables compatible with the Xilinx Vivado and enable developers to implement video frame grabbers in a plug-and-play manner.

Xylon provides a number of free downloadable logicBRICKS reference designs to enable risk-free IP core evaluations and jump-start new developments. For example, the logiREF-MEDIA-ZED pre-verified reference design for the ZedBoard kit demonstrates video frame grabbing, audio recording and playback, and design of Graphics Human Machine Interfaces (HMI) under the Linux operating system:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Multimedia-for-Zynq-AP-SoC-ZedBoard.aspx

Functional Description

The logiWIN internal structure is shown on the block diagram on Figure 1. The logiWIN functional blocks are:

Input Selector

Input Selector instantiates input channel mux (if two inputs are enabled) and different re-formatters (AXIS2Parallel, YUV 4:2:2 to 4:4:4, …) and color converters (YUV2RGB, RGB2YUV,…). Type of re-formatter and color converter depends on input and output types.

Input Sampler

Video input stream is synchronized to corresponding video input clock. Input Sampler block re-samples the video input so it is synchronized to video memory clock or video output stream clock. Re-sampled data and clock are driven as input to the Scaler block

Timing Analyzer

Timing Analyzer measures horizontal and vertical resolutions at selected video input and at video input clock. Results are stored in corresponding registers; it can be useful for debugging and testing purposes.

Scaler

The Scaler uses the bilinear interpolation for up and down scaling of the input video resolution. The input video can be zoomed in 64 times (scale up 64x), or zoomed out 16 times (scale down 1/16). This scaling range is quite wide, but needs to be carefully used in order to preserve the image quality. The video resolution can be maximally scaled down two times without image quality losses. Further high-quality lossless scaling down is possible in the logiWIN cascade scaling mode.

The Scaler block can also crop the image in both vertical and horizontal direction.

Output Buffer

The Output Buffer is instantiated if stream output is disabled. It is used to store resulting image to memory.

The Output Buffer consists of three main parts: Memory Address Generator, AXI4 Master interface and part which handles double/triple buffering.

Memory Address Generator calculates address for each burst transfer, depending on selected output type, row stride, memory base address, memory address offset, output image positioning and type of de-interlacing and swizzling (if in use).

Double/triple buffering is implemented in order to remove flicker, shearing, and tearing artifacts. Buffer offset is defined in number of lines; using buffer offset generic parameter or register.

Stream Out

The “Stream Out” module is instantiated if AXIS video stream output or Parallel video output is enabled. This accepts data from scaler and generates video data stream and control signals for selected output stream interface.

AXI Registers

All logiWIN registers are instantiated in this block. The CPU has access to all these registers through the AXI4-Lite bus.

Core Modifications

The core is supplied in an encrypted VHDL format which allows the user to take a full control over configuration parameters. Table 2 outlines the most important logiWIN configuration parameters selectable prior to the VHDL

synthesis. For a complete list of parameters, please consult the logiWIN User's Manual delivered with the IP core.

Table 2: logiWIN VHDL Configuration Parameters

Parameter	Description
C_NUM_OF_INPUTS	Number of video inputs
C_INPUT_SMPL_PER_CLOCK	Video input number of pixels per clock.
C_USE_S_AXIS_0	Channel 1 stream type: 1 – AXIS Video, 0 – Parallel video
C_S_AXIS_0_FORMAT	Channel 1 AXIS input type: RGB, YUV4:2:2, YUV4:4:4, Y (Mono)
C_INPUT_0_TYPE	Channel 1 video input type: RGB, YUV4:2:2, YUV4:4:4, Y (Mono)
C_USE_S_AXIS_1	Channel 2 stream type: 1 – AXIS Video, 0 – Parallel video
C_S_AXIS_1_FORMAT	Channel 2 AXIS input type: RGB, YUV4:2:2, YUV4:4:4, Y (Mono)
C_INPUT_1_TYPE	Channel 2 video input type: RGB, YUV4:2:2, YUV4:4:4, Y (Mono)
C_YUV_BITS	Number of YUV bits. Valid values are 8 bits or 16 bits
C_OUTPUT_TYPE	Video output type: RGB565, RGB888, ARGB6565, ARGB8888, YUV4:2:2, YUV4:4:4, Y (Mono)
C_USE_M_AXIS	AXI video stream video output: 0 – disable, 1 – enable
C_M_AXIS_FORMAT	AXI Video stream output format: YUV4:2:2, YUV4:4:4, RGB, RGBA, Mono(Y)
C_USE_VDATA_OUT	Parallel video output: 0 – disable, 1 – enable
C_USE_COLOR_MANAGEMENT	Includes or excludes color enhancement module for ITU or YUV input
C_CONVERTER_USE_MULTIPLIER	Defines type of multipliers in color space converters
C_CASCADE_ON	Enables cascaded scaling for lossless scale-down operations
C_USE_XSCALE	Horizontal scaling implementation on/off
C_USE_YSCALE	Vertical scaling implementation on/off
C_USE_PLANES	Use planar memory storing method.

The logiWIN has been constructed with regard to adaptability to various cameras and other video input sources. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiWIN core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiWIN to your requirements. The logiWIN source code is available at additional cost from Xylon.

Core I/O Signals

The core I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
interrupt	Output	Interrupt signal, level sensitive, active high
Memory Interface		
AXI4 Master Interface	Bus	ARM AMBA AXI4 master interface
Register Interface		
AXI4-Lite Slave Interface	Bus	AMBA AXI4-Lite slave interface
Video Input Interfaces and Signals		
s_axis_0 AXI4-Stream Slave Interface	Bus	Channel1: ARM AMBA AXI4-Stream Slave video interface
s_axis_1 AXI4-Stream Slave Interface	Bus	Channel2: ARM AMBA AXI4-Stream Slave video interface
vclk_in	Input	Video input clock used for both channels if C_USE_EXT_CLOCKING = 1. This is valid for both video input types (parallel and AXIS).
vclk_in_sel	Output	Video input clock select, CTRL0_REG bit 4
vclk_0	Input	Channel1: video input clock
vdata_in_0[C_INPUT_SMPL_PER_CLOCK*24-1:0]	Input	Channel1: video input data
vdata_in_de_0	Input	Channel1: data enable (use only for RGB and YUV input types), must be active during one video line
vdata_in_de_vld_0	Input	Channel1: data enable valid, used as clock enable during data valid period
vdata_in_hs_0	Input	Channel1: hsync
vdata_in_vs_0	Input I	Channel1: vsync
vdata_in_fld_0	Input	Channel1: field
vdata_in_rdy_0	Output	Channel1: ready, used to stall input stream
vdata_in_rdy_fb_0	Input	Channel1: ready feedback
vclk_1	Input	Channel2: video input clock
vdata_in_1[C_INPUT_SMPL_PER_CLOCK*24-1:0]	Input	Channel2: video input data
vdata_in_de_1	Input	Channel2: data enable, must be active during one video line
vdata_in_de_vld_1	Input	Channel2: data enable valid, used as clock enable during data valid period
vdata_in_hs_1	Input	Channel2: hsync
vdata_in_vs_1	Input	Channel2: vsync
vdata_in_fld_1	Input	Channel2: field
vdata_in_rdy_1	Output	Channel2: ready, used to stall input stream
vdata_in_rdy_fb_1	Input	Channel2: ready feedback
Video Output Interfaces and Signals		
m_axis AXI4-Stream Master Interface	Bus	ARM AMBA AXI4-Stream Master video interface
vdata_out_clk	Input	Video output clock
vdata_out_rst	Input	Video output reset, synchronous, active high.
vdata_out [C_VDATA_OUT_WIDTH-1:0]	Output	Video output data
vdata_out_vs	Output	Video output vsync
vdata_out_de	Output	Video output data enable, active when data at vdata_out bus is valid
vdata_out_field	Output	Video output field

Signal	Signal Direction	Description
vdata_out_last	Output	Video output last, active with last pixel in line
vdata_out_rdy	Input	Video output ready, used to stall output stream
Auxiliary Signals		
curr_vbuff[1:0]	Output	Triple buffering: current video memory buffer
next_vbuff[1:0]	Input	Triple buffering: next video memory buffer to write to
sw_vbuff_req	Output	Triple buffering: request for buffer switching
sw_vbuff_grant	Input	Triple buffering: buffer switching granted
rst_regs	Input	Synchronous, active high register reset. Resets registers to default values.
fifo_error	Output	Active (logic high) when any of the FIFOs' error occurs. Remains active until vertical synchronization signal arrives
capture_stop	Input	Image capture stop signal

Verification Methods

The logiWIN is fully supported by the Xilinx Vivado (IPI) Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiWIN implementation does not require any particular skills beyond general Xilinx tools knowledge. The IP core version packaged for the Xilinx Vivado Design Suit is shipped with compiled simulation libraries for ModelSim simulator from Mentor Graphics. For information about Vivado compatible IP core simulations, please contact Xylon.

The logiWIN evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

http://www.logicbricks.com/Products/logiWIN.aspx

Recommended Design Experience

The user should have experience in the following areas:

- **Xilinx design tools**
- **ModelSim**

Available Support Products

The pre-verified MPSoC Multi-Camera Vision kits from Xylon presents logicBRICKS IP cores for video capturing and processing of the video data under the Linux operating system running on the Xilinx Zynq-7000 SoC and Zynq UltraScale+ MPSoC based Xilinx Development Kits. Xylon's vision kits provide system designers with everything they need to efficiently develop multi-camera vision applications for the automotive and other embedded markets:

URL: **https://www.logicbricks.com/Solutions/Xylon-MPSoC-Vision-Development-Kit.aspx**

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.02.	12.03.2009.	Initial Xylon release – new doc template.
2.03.	27.03.2009.	Added VCLK_IN and VCLK_IN_SEL signals to the Table 3: Core I/O Signals.
2.05.	15.03.2010.	Updated Table 1 and Table 3.
2.05.	06.04.2010.	New doc template.
2.06.	07.07.2010.	Document name changed.
2.07.	31.12.2010.	Added RGB to YCrCb converter to Features and Figure 1: logiWIN Architecture.
3.01	23.11.2011.	Added YUV 4:2:2 input, including YUV to RGB converter and color enhancement block. Added AXI4 Master interface for memory access and AXI4-Lite Slave interface for registers.
3.02	17.07.2012.	Byte swapping option added for register and memory bus interface. Endianness correction removed for registers layout. Color format order in output pixel format selectable between: ARGB and ABGR, as well as between CrY2CbY1 <-> Y2CrY1Cb.
4.00	29.01.2014.	Removed OPB and PLB busses. Added field signal on both video inputs.
4.01	23.09.2014.	Updated Table 1 and Table 3. Added capture_stop input signal. Added fifo_error output signal. Added default register settings. Scaler module optimized for better routing.
4.1	26.11.2014.	IP core version naming convention modified for Vivado IP-XACT package compliance. Patch level designation is replaced by IP core's revision tag.
4.2	30.10.2015.	Corrected description of C_YUV_BITS generic parameter in Table 2 Corrected input signals' description in Table 3. IP core prepared for Vivado 2015.2.
4.2	26.10.2016.	Added utilization information for Zynq® UltraScale+™ XCZU9EG-1 MPSoC. Updated Table 1.
5.0	18.12.2017.	Added stream inputs and outputs. Added new features to features list Updated logiWIN Architecture. Updated Figure 1, Table 1, Table 2 and Table 3.
5.0	20.11.2019.	Updated FPGA resource utilization information in Table 1.
5.1	17.12.2019.	Updated Features section. logiWIN supports maximum input and output resolution of 4096x4096 pixels.
5.2	06.02.2020.	Added support for Versal ACAP. Updated Table 1.
6.1.	28.02.2023.	Removed ITU inputs. Removed memory interfaces, only AXI4 memory interface is used. Added multiple pixel per clock support for input video, 2 and 4 pixels per clock is now supported. Added support for addressing more than 4GB of video memory. Support for packed RGB added (TRUERGB888 3BPP). Added semiplanar support for RGB888, YUV444 and YUV422 formats. Added linear memory storage support. Maximum input/output resolution up to 8K.