logiISP-2A Software Library Bundle for the logiISP-UHD Image Signal Processing IP Core

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Software Facts

Provided with the Library Bundle	
Included Libraries	Auto-White Balance (AWB Library) Auto-Exposure (AE Library)
Documentation	logiISP-UHD User's Manual Separate doxygen files for each library with a simple library usage examples
File Format	Pre-Compiled Static Library (.a type)
Verification/Validation	Simulated and HW validated
Reference Designs & Application Notes	Available. Please contact Xylon.
Additional Available Items	logiISP-ZU-GMSL2 Evaluation Kit logiVID-ACAP-ISP Evaluation Kit MPSoC and ACAP reference designs
Support	
Support provided by Xylon (E-Mail)	

Features

- Licensable software libraries for real-time camera Auto-White Balance (AWB) and Auto-Exposure (AE) for use with the logiSP-UHD Image Signal Processing IP Core
- Provided as separate pre-compiled files (binaries) but sold together as a library bundle (logiISP-2A)
- Processor-based control algorithms intended for implementation on the ARM® CPU and AMD-Xilinx MicroBlaze Soft Processor Core
- Possibility of compiling the libraries for other computer architectures on customer request
- Supports AMD-Xilinx Versal® ACAPs, Zynq®-7000 SoCs, Zynq UltraScale+™ MPSoCs, UltraScale™.UltraScale+ and 7-Series FPGA devices
- The libraries work in conjunction with the logiISP-UHD IP Core and require the Image Statistics (STATS) logiISP-UHD block to be implemented into the working hardware ISP pipeline for full functionality
- AWB has the option to calculate the gains in the sensor itself, and therefore avoiding the need to use the Color Correction Matrix (CCM) block
- The libraries access image statistics data collected by the STATS block through the AMBA® AXI4-Lite Control Interface simply by reading STATS registers and BRAMs
- Pre-processed statistics data is handed over to the processor at the end of each frame for analysis
- Can access the sensor configuration registers through I2C or SPI serial bus for reprogramming
- High-Dynamic Range (HDR) operation mode is possible in combination with Xylon's logiHDR IP core
- Support for resolutions up to 7680x7680, including UHD 4K2Kp60 (3840x2160@60fps)
- Library deliverables include the library itself, documentation and technical support

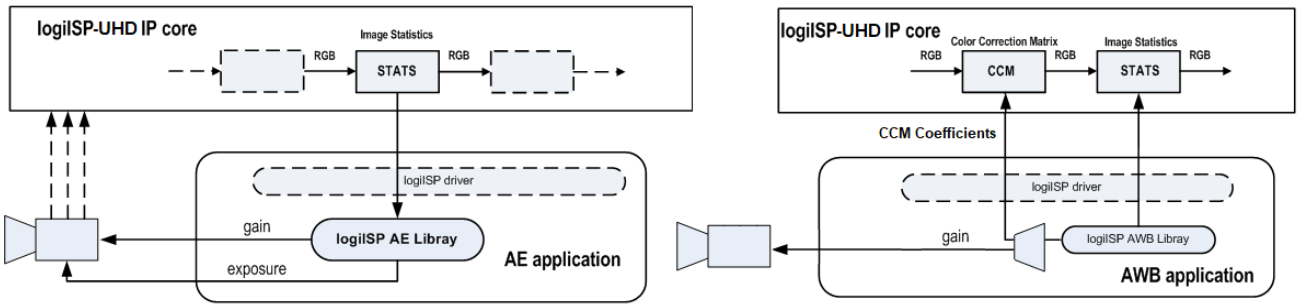

Figure 1: Software Libraries and the logiISP-UHD IP in operation – Example Block Diagram

Applications

Application fields include Surveillance, Automotive Driver Assist, Machine Vision, Video Conferencing, Digital Signage, Medical Imaging, Aerospace and Defense, and others.

General Description and Usage Example

Assuming a user has an image sensor for which it requires Defective Pixel Correction, Auto White Balancing (AWB) and Auto Exposure (AE) implementation. It also requires the output of the processing chain to be in RGB video format. The processed image needs to be stored to external memory.

Figure 2 provides an outline of a simplified SoC architecture for fulfilling user requirements. PL stands for Programmable Logic, and PS for Processing System.

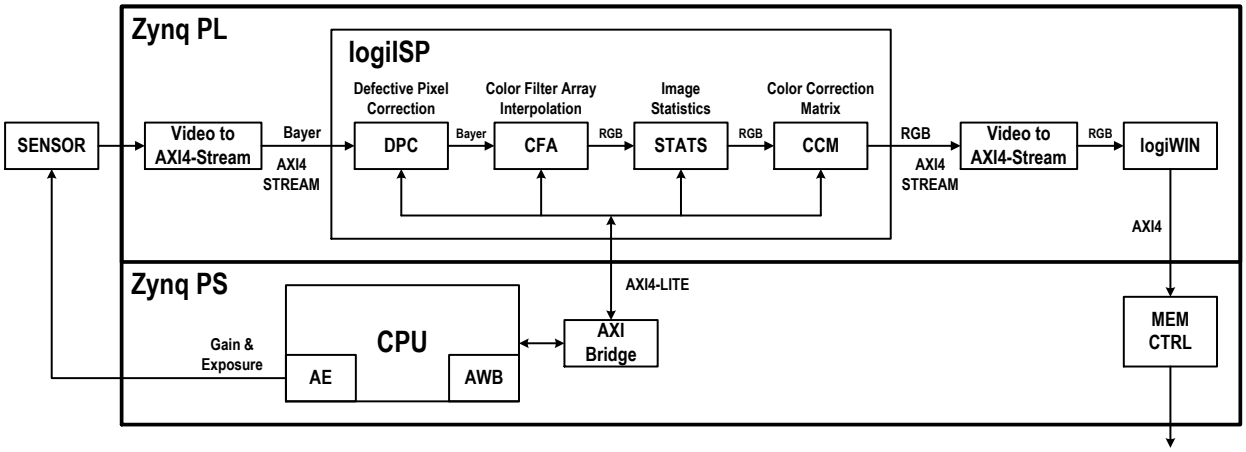

Figure 2: Example logiISP-UHD IP Core Configuration

On the input to SoC programmable logic we have a Bayer stream coming from a sensor and entering the logiISP-UHD IP core. The first block in the logiISP-UHD is the Defective Pixel Correction block that performs real-time detection and correction of defective pixels in a camera image sensor array.

In order to implement the AWB and AE algorithms the logiISP-UHD pipeline includes Image Statistics (STATS) and Color Correction Matrix (CCM) blocks.

However, as the STATS block can only work with the RGB video format on its input, the corrected Bayer stream needs to be converted into a full RGB video format. For that reason the logiISP-UHD pipeline includes a Color Filter Array Interpolation (CFA) block in front of the STATS block. The CFA block reconstructs sub-sampled color data for images captured by a Bayer Color Filter Array image sensor and outputs full RGB data for each input pixel.

The STATS block generates statistical data for color histograms, mean and variance values, edge and frequency content for 64 user-defined zones on a per frame basis. Statistical information collected by the STATS block can now be used in control algorithms for the AWB and AE algorithm. In the proposed system architecture the AWB and AE are algorithms implemented on ARM CPU available in the AMD-Xilinx Zynq All Programmable SoC.

The algorithms can access image statistics data collected by the STATS block through the AXI4-Lite control interface by simply reading STATS registers and BRAMs. Pre-processed statistics data is handed over to the processor at the end of each video frame for analysis.

After analysis, the AE algorithm can access sensor configuration registers through the I2C, SPI or similar communication channel, and reprogram the exposure and gain settings in accordance with the calculated values.

In a similar way, the AWB algorithm can access the CCM block implemented in the logiISP-UHD IP core and correct output colors by reprograming the color correction matrix. The CCM block generates the requested RGB formatted video output.

The AXI4-Stream data coming out of the logiISP-UHD IP core can then be connected to the logiWIN Versatile Video Input IP core and streamed to external memory. The logiWIN and logiISP-UHD IP cores are part of Xylon's popular logicBRICKS library of IP cores.

Functional Description

The logiISP-UHD IP Core's functional blocks that are relevant to the proper functioning of the logiISP-2A libraries are as follows:

Color Filter Array Interpolation (CFA)

The Color Filter Array Interpolation block reconstructs sub-sampled color data from images captured by a Bayer Color Filter Array image sensor. Such sensors measure the intensity of one principal color at any pixel location and the CFA block converts them to an RGB formatted video output.

Image Statistics (STATS)

The Image Statistics block implements the computationally intensive metering functionality common in digital cameras, camcorders and imaging devices. The STATS block generates a set of statistics for color histograms, mean and variance values, edge and frequency content for 64 user-defined zones on a per frame basis. Statistical information can be used with different processor-based control algorithms. Auto-White Balance (AWB) and Auto-Exposure (AE) software libraries can be licensed from Xylon.

Color Correction Matrix (CCM)

The Color Correction Matrix block corrects image color variations caused by different conditions that can include spectral characteristics of the optics (lens, filters), lighting source variations, characteristics of the color filters of the sensor and many others. The CCM block contains 3x3 programmable coefficient matrix multipliers with offset compensation that can be used in color correction operations such as adjusting white balance, color cast, brightness, or contrast in an image.

Recommended Design Experience

The user should have experience in the following areas:

- logiISP-UHD IP Core Architecture
- Camera systems
- ANSI C Programming

Available Support Products

The logiHDR is an Ultra High Definition (UHD) HDR pipeline designed for digital processing and image quality enhancements of raw image data from HDR sensors. The logiHDR works in combination with the logiISP-UHD IP core to extract maximum detail from high-contrast scenes, i.e. scenes with objects highlighted by direct sunlight and objects placed in extreme shades:

URL: https://www.logicbricks.com/Products/logiHDR.aspx

The logiISP-ZU-GMSL2 HDR ISP Evaluation Kit provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to develop multi-camera vision applications on AMD-Xilinx's Zynq UltraScale+ MPSoC devices. The complete hardware platform includes Xylon's 12-Ch GMSL2 FMC Daughter Card, four of Xylon's 2.3MP automotive video cameras with the raw Bayer video output and it supports the HDMI video output. Kit deliverables include the logiREF-MULTICAM-ISP reference design that demonstrates parallel HDR ISP processing of four video inputs.

URL: https://www.logicbricks.com/Solutions/Xylon-HDR-ISP-Pipeline.aspx

The logiVID-ACAP-ISP HDR ISP Evaluation Kit for Versal ACAP provides system designers with everything they need to evaluate Xylon's logicBRICKS HDR ISP Suite and to develop multi-camera vision applications on AMD-Xilinx's Versal ACAP devices. The complete hardware platform includes three Leopard Imaging Ultra High-Definition automotive video cameras, Xylon's 12-Ch GMSL2 FMC Daughter Card and it supports the HDMI video output. Kit deliverables include the logiREF-ACAP-MULTICAM-ISP reference design that demonstrates parallel HDR ISP processing of three UHD video inputs. The Versal AI Core Series VCK190 Evaluation Kit is not included in the kit and should be sourced separately.

URL: https://www.logicbricks.com/HDR-ISP-KIT-Versal-ACAP.aspx

Ordering Information

This product is available directly from Xylon under the terms of Xylon's IP License. Please contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

AMD-Xilinx Programmable Logic

For information on AMD-Xilinx programmable logic or development system software, contact your local AMD sales office, or:

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Revision History

Version	Date	Note
1.0	November 25th, 2022	Initial release of the document.